Michal Sojka
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March 13, 2017
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- Mutual exclusion (e.g. access to shared data)
- Producer-consumer (e.g. database waits for requests)
Synchronization

- **Multi-core** CPUs are today’s norm, many-core CPUs will come tomorrow.
- To take advantage of such a hardware, parallel (multi-threaded) programs must be run on them.
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  - ...


Outline

1. Naive synchronization
   - Problems

2. Semaphores

3. Futex

4. Real-mostly workload

5. Read-Copy-Update (RCU)
   - RCU implementations
Data should be modified at most by one thread at a time:

```cpp
bool locked;

void func() {
    while (locked == true)
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Naive synchronization
Mutual exclusion

Terminology: code in the “locked” region is called critical section

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6. Busy waiting wastes energy
Atomic operations

- C: `data++
- Assembler (x86): `inc ($data)` – uninterruptible
- Hardware: memory bus read, ALU, memory bus write

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<thead>
<tr>
<th>CPU0</th>
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<tbody>
<tr>
<td>bus read</td>
<td></td>
<td>0</td>
</tr>
<tr>
<td>ALU</td>
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<td>0</td>
</tr>
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Atomic operations ensure that the operation (typically read-modify-write) is atomic (uninterruptible) even at the hardware (bus) level.
- `compare-and-swap/CAS` instruction (x86: `cmpxchg`)
Atomic operations

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- **compare-and-swap/CAS instruction (x86: cmpxchg)**

```c
void lock() {
    while (locked == true) {
        /* busy wait */;
        locked = true;
    }
}
```

```c
void lock() {
    while (__atomic_exchange_n(&locked, true, ...
                               ) == true) {
        /* busy wait */;
    }
}
```
bool locked;

while (locked)
{
}
locked = true;
data++;
locked = false;

Compiler expects the memory is only modified by the program being compiled
Locked seems to be useless ⇒ optimize out
bool locked;

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Locked seems to be useless ⇒ optimize out
Compiler is free to reorder operations as long as the result of the computation is the same
Compiler optimizations

```c
bool locked;

while (locked)
{
}
locked = true;
data++;
locked = false;
```

```c
#define barrier() \
    asm volatile("" : : : "memory"
volatile bool locked;

while (locked)
{
}
locked = true;
barrier();
data++;
barrier();
locked = false;
```

- Compiler expects the memory is only modified by the program being compiled
- Locked seems to be useless ⇒ optimize out
- Compiler is free to reorder operations as long as the result of the computation is the same
Defining the variable volatile makes all accesses “volatile” i.e. slow.

Sometime, we need volatile only certain accesses and the rest can be optimized:

```c
#define ACCESS_ONCE(x) (*(volatile typeof(x) *)&(x))
#define LOAD_SHARED(p) ACCESS_ONCE(p)
#define STORE_SHARED(x, v) ({ ACCESS_ONCE(x) = (v); })
#define barrier() asm volatile("" : : : "memory")
```
## Hardware reordering

- Different CPU architectures implement different memory consistency models
- Some operations can be reordered with respect to other operations

<table>
<thead>
<tr>
<th>Type</th>
<th>Alpha</th>
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- x86 can reorder stores after loads, i.e. data can be read before other CPUs see locked set to true!
- Why? Stores may have to wait for cache-line ownership. Not waiting with subsequent reads improves performance.
- Solution: Insert memory barrier instructions.
  - e.g. mfence on x86
  - C11/C++11 atomics allow to specify which ordering has to be maintained
### Cost of atomic operations & barriers

16-CPU 2.8GHz Intel X5550 (Nehalem) System

<table>
<thead>
<tr>
<th>Operation</th>
<th>Cost (ns)</th>
<th>Ratio</th>
</tr>
</thead>
<tbody>
<tr>
<td>Clock period</td>
<td>0.4</td>
<td>1.0</td>
</tr>
<tr>
<td>“Best-case” CAS</td>
<td>12.2</td>
<td>33.8</td>
</tr>
<tr>
<td>Best-case lock</td>
<td>25.6</td>
<td>71.2</td>
</tr>
<tr>
<td>Single cache miss</td>
<td>12.9</td>
<td>35.8</td>
</tr>
<tr>
<td>CAS cache miss</td>
<td>7.0</td>
<td>19.4</td>
</tr>
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<td>Single cache miss (off-core)</td>
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<td>86.6</td>
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<td>CAS cache miss (off-core)</td>
<td>31.2</td>
<td>86.5</td>
</tr>
<tr>
<td>Single cache miss (off-socket)</td>
<td>92.4</td>
<td>256.7</td>
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Source: Paul E. McKenney, IBM

- Barriers are typically cheaper (weak barriers more than full barriers)
Cost of atomic operations & laws of physics

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Interconnect

Memory

Interconnect

- Speed of light: RT in 1 cycle @ 3 GHz = 5 cm
- Speed of electrons in transistors: 0.03–0.3 C

All CPUs executing atomic increment of global variable
Cost of atomic operations & laws of physics

Speed of light RT in 1 cycle @ 3 GHz = 5 cm
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All CPUs executing atomic increment of per-cpu variable

10/35
Cost of atomic operations & laws of physics

All CPUs executing atomic increment of per-cpu variable

- Speed of light RT in 1 cycle @ 3 GHz = 5 cm
- Speed of electrons in transistors: 0.03–0.3C
Locking overhead

Single-instruction critical sections protected by multiple locks

Uncontended

256.7 cycles

1 cycle

Contended, No Spinning

256.7 cycles

1 cycle

256.7 cycles
Deadlock

Example:
- Single-core system
- Two threads low- and high-priority

```
LP_thread       HP_thread
~~~~~~~~~~~~~~  ~~~~~~~~~
lock();         lock();
data++;          data++;
→ preemption    →
    deadlock();
```
Deadlock

- **Example:**
  - Single-core system
  - Two threads low- and high-priority

```
LP_thread        HP_thread
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lock();
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    →  preemption →
  deadlock();
```

- **Solution:** When the lock is not available, ask the OS scheduler to put your thread to sleep and wake you up after the lock is available
  - Problem: atomicity of checking the lock and going to sleep
  - Requires implementation in the OS kernel
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   - RCU implementations
Each system call adds overhead (≈ 100 cycles on modern HW)

- It is preferable to use “fine-grain” locking, i.e. locks protect as little data as possible to prevent lock contention.

- If fine-grain locking is effective the lock is not contended and threads rarely have to sleep, but always pay the syscall overhead!

- That’s not efficient – the solution in Linux is called **futex**.
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Futex

Fast Userspace Mutex

- Uncontended mutex never goes to kernel
- It uses atomic instruction `cmpxchg(val, expct, new) \rightarrow prev`
- `futex_wait()` and `futex_wake()` are system calls

```cpp
class mutex {
    public:
        mutex () : val (0) { } 
        void lock () {
            int c;
            if ((c = cmpxchg (val, 0, 1)) != 0) {
                if (c != 2)
                    c = xchg (val, 2);
                while (c != 0) {
                    futex_wait (&val, 2);
                    c = xchg (val, 2);
                }
            }
        }
        void unlock () {
            if (atomic_dec (val) != 1) {
                val = 0;
                futex_wake (&val, 1);
            }
        }
    private:
        int val;
};
```

Futex uses

- Mutexes
- Semaphores
- Conditional variables
- Thread barriers
- Read-write locks
The problem of mutex

Mutual exclusion in read-mostly workload

CPU 0

Reader

CPU 1

CPU 2

Reader

Dead Time!!!

Reader

CPU 3

Updater
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Real-mostly workload

Read-Write lock

- Update blocks readers
- Can be implemented on top of mutex(es)
We want this

- Updater does not block readers
- Is that possible?
Read-Copy-Update (RCU)

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- Read-side scalability of various synchronization primitives
- RCU is **scalable** – typically up to hundreds or thousands of CPUs
Read-side scalability of various synchronization primitives

- RCU is **scalable** – typically up to hundreds or thousands of CPUs
- Locking does **not scale**
1. Original list
Updating RCU-based list

1. Original list
2. Copy B
Updating RCU-based list

1. Original list
2. Copy B
3. Update B to D
Updating RCU-based list

1. Original list
2. Copy B
3. Update B to D
4. Make the updated element visible to readers
Updating RCU-based list

1. Original list
2. Copy B
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5. Wait after all readers stop accessing B and free it
Main mechanisms of RCU

1. Publishing of updates (3→4)
   - Ensure that updated data reach memory before the updated pointer
   - Compiler and memory barrier
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1. Publishing of updates (3→4)
   - Ensure that updated data reach memory before the updated pointer
   - Compiler and memory barrier

2. Accessing new versions of data (how readers traverse the list)
   - Ensure that we see all the updates made before publishing
   - Compiler and memory barrier
Main mechanisms of RCU

1. Publishing of updates (3→4)
   - Ensure that updated data reach memory before the updated pointer
   - Compiler and memory barrier

2. Accessing new versions of data (how readers traverse the list)
   - Ensure that we see all the updates made before publishing
   - Compiler and memory barrier

3. Waiting for all readers to finish
Main mechanisms of RCU

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2. Accessing new versions of data (how readers traverse the list)
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3. Waiting for all readers to finish
   - The tricky part!
   - No explicit (and expensive) tracking of each reader
   - RCU uses indirect way of determining the end of all read-side sections
   - In certain implementations (QSBR) read-side has zero overhead
Read-Copy-Update (RCU)

RCU concepts and API

Reader  Reader  Reader  Reader
Reader  Reader  Reader  Reader
Reader  Reader  Reader  Reader
Reader  Reader  Reader  Reader
Reader  Reader  Updater  Free
RCU concepts and API

Read-side critical section
rcu_read_lock()/unlock()

Reader Reader Reader Reader

Reader Reader Reader Reader

Reader Reader Reader Reader

Reader Reader Updater Free
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Reader Reader Reader Reader

rcu_dereference()

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code outside r.s.c.s.

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rcu_assign_pointer()
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rcu_assign_pointer()

Grace period
started and waited by synchronize_rcu()
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Quiescent state
code outside r.s.c.s.

rcu_dereference()

Must not happen!

rcu_assign_pointer()

Grace period
started and waited by synchronize_rcu()
rcu_read_lock(); /* Start critical section. */

p = rcu_dereference(cptr);
/* *p guaranteed to exist. */
do_something_with(p);
rcu_read_unlock(); /* End critical section. */
/* *p might be freed!!! */

- rcu_read_lock()/unlock() and rcu_dereference() are cheap, sometimes *nop*.
- Updaters are more heavy-weight.


```c
pthread_mutex_lock(&updater_lock); /* not needed if there is just one updater */
old_p = cptr; /* copy if needed */
rcu_assign_pointer(cptr, new_p); /* update */
pthread_mutex_unlock(&updater_lock);
synchronize_rcu(); /* Wait for grace period */
free(old_p);
```
How does it work?

- Many implementations possible
- Trade-off between read-side overhead and constraints of application structure
Quiescent-state based reclamation (QSBR)

// Protects registry from concurrent accesses
pthread_mutex_t rcu_gp_lock =
   PTHREAD_MUTEX_INITIALIZER;

LIST_HEAD(registry);

struct rcu_reader {
   unsigned long ctr;
   char need_mb;
   struct list_head node;
   pthread_t tid;
};

/* per-thread variable */
struct rcu_reader __thread rcu_reader;

void rcu_register_thread(void) {
   rcu_reader.tid = pthread_self();
   mutex_lock(&rcu_gp_lock);
   list_add(&rcu_reader.node, &registry);
   mutex_unlock(&rcu_gp_lock);
   rcu_thread_online();
}

void rcu_unregister_thread(void) {
   rcu_thread_offline();
   mutex_lock(&rcu_gp_lock);
   list_del(&rcu_reader.node);
   mutex_unlock(&rcu_gp_lock);
   rcu_thread_online();
}

#define RCU_GP_ONLINE 0x1
#define RCU_GP_CTR 0x2

// global counter
unsigned long rcu_gp_ctr = RCU_GP_ONLINE;

static inline void rcu_read_lock(void) {}
static inline void rcu_read_unlock(void) {}

/* Every thread must call this function periodically
 * outside of read-side critical section.
 */
static inline void rcu_quiescent_state(void) {
   smp_mb();
   STORE_SHARED(rcu_reader.ctr, LOAD_SHARED(rcu_gp_ctr));
   smp_mb();
}

/* call before blocking system call */
static inline void rcu_thread_offline(void) {
   smp_mb();
   STORE_SHARED(rcu_reader.ctr, 0);
}

/* call after return from blocking system call */
static inline void rcu_thread_online(void) {
   STORE_SHARED(rcu_reader.ctr, LOAD_SHARED(rcu_gp_ctr));
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}
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    STORE_SHARED(rcu_reader.ctr,
        LOAD_SHARED(rcu_gp_ctr));
    smp_mb();
}
```

Properties:

- Grace periods are not shared
- Long waiting $\Rightarrow$ higher memory consumption
- Works only on 64-bit architectures – the counter must not overflow
General-purpose RCU

Properties:
- Does not restrict application structure
- Higher read-side overhead (still less than typical locks).

```c
#define RCU_GP_CTR_PHASE 0x10000
#define RCU_NEST_MASK 0x0ffff
#define RCU_NEST_COUNT 0x1

unsigned long rcu_gp_ctr = RCU_NEST_COUNT;

static inline void rcu_read_lock(void) {
    unsigned long tmp;
    tmp = rcu_reader.ctr;
    if (!(tmp & RCU_NEST_MASK)) {
        STORE_SHARED(rcu_reader.ctr, LOAD_SHARED(rcu_gp_ctr));
        smp_mb();
    } else {
        STORE_SHARED(rcu_reader.ctr, tmp + RCU_NEST_COUNT);
    }
}

static inline void rcu_read_unlock(void) {
    smp_mb();
    STORE_SHARED(rcu_reader.ctr, rcu_reader.ctr - RCU_NEST_COUNT);
}
```
void synchronize_rcu(void)
{
    smp_mb();
    mutex_lock(&rcu_gp_lock);
    update_counter_and_wait();
    barrier();
    update_counter_and_wait();
    mutex_unlock(&rcu_gp_lock);
    smp_mb();
}

static void update_counter_and_wait(void)
{
    struct rcu_reader *index;
    STORE_SHARED(rcu_gp_ctr, rcu_gp_ctr \ RCU_GP_CTR_PHASE);
    barrier();
    list_for_each_entry(index, &registry, node) {
        while (rcu_gp_ongoing(&index->ctr))
            msleep(10);
    }
}

static inline int rcu_gp_ongoing(unsigned long *ctr)
{
    unsigned long v;
    v = LOAD_SHARED(*ctr);
    return (v & RCU_NEST_MASK) && ((v \ rcu_gp_ctr) & RCU_GP_CTR_PHASE);
}
Update benchmarks

Fig. 9. Update Overhead, 8-core Intel Xeon, Logarithmic Scale

Fig. 10. Update Overhead, 64-core POWER5+, Logarithmic Scale

Fig. 11. Impact of Update-Side Critical Section Length on Read-Side, 8-core Intel Xeon, Logarithmic Scale

Fig. 12. Impact of Update-Side Critical Section Length on Read-Side, 64-core POWER5+, Logarithmic Scale
Conclusion

- RCU is scalable synchronization mechanism for hundreds/thousands of CPUs and read-mostly workload
- We have seen a RCU-based implementation of single-linked list, but many other common data structures can implemented in RCU-compatible way

References