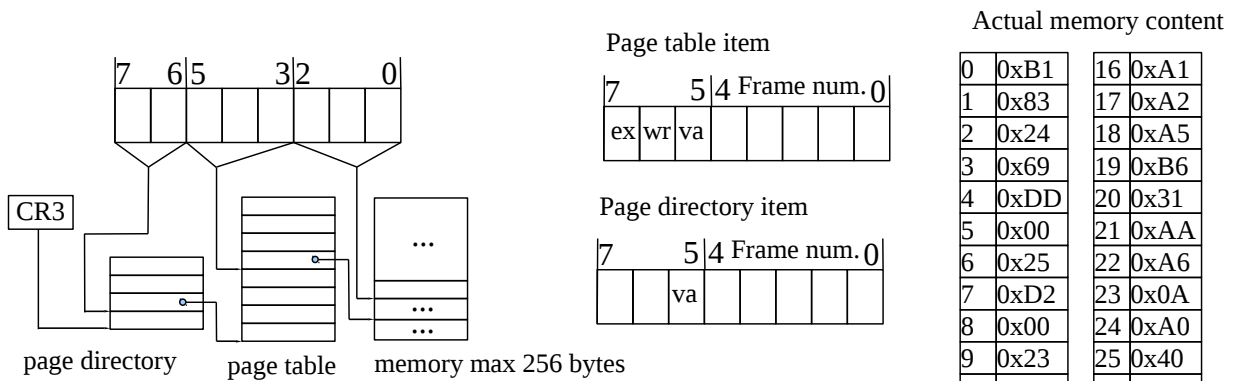


Suppose we have a system with 8-bit address bus. Size of page is 8 bytes and two level hierarchical paging is used. Register CR3 defines frame with page directory, two most significant bits define position in the page directory that points to frame with page table. Bits 3-5 defines position in page table. Item in page table contains 5-bits of frame in memory and bits: *va* – 1=valid/0=invalid, *wr* – write 1=enable/0=disable, *ex* – execute 1=enable/0=disable. Item from page directory contains 5 bits of frame with page table and bit *va* – 1=valid/0=invalid.



Actual memory content is described in right part and the register CR3 has value 1.

Define content of memory with logical address 0x42 (binary 01 000 010)?

Is it possible to modify or execute this memory cell?

Define content of memory with logical address 0x49 (binary 01 001 001)?

Is it possible to modify or execute this memory cell?

Define content of memory with logical address 0x53 (binary 01 010 011)?

Is it possible to modify or execute this memory cell?

Which pages from LA are in memory? What happens if CPU asks for address that is not in memory?

### Virtual memory – paging

Process P can use only 4 frames of memory and is using these pages: 1,2,3,4,5,3,2,5,1,2,5,4. How many page faults there will be using FIFO, LRU, or Second chance algorithm? What is the minimal number of page faults for this sequence? Draw diagram that shows usage of memory.

### Working set

3 processes use following pages:

P1	1	1	2	1	2	3	4	3	4	5	1	5	1	5	1	5	1	2	1
P2	10	10	10	10	11	12	13	10	11	12	13	10	11	12	13	10	11	12	13
P3	20	21	22	21	21	20	22	21	23	24	25	20	21	22	25	20	21	22	20
WS	-	-	-																
Sizes																			

Suppose that the working set has window with 4 time units (4 columns in table). Fill how many pages is used by these 3 processes for each time. Fill optimal distribution of memory to processes and explain why? Can there be a thrashing if the size of real-memory is only 9 frames.