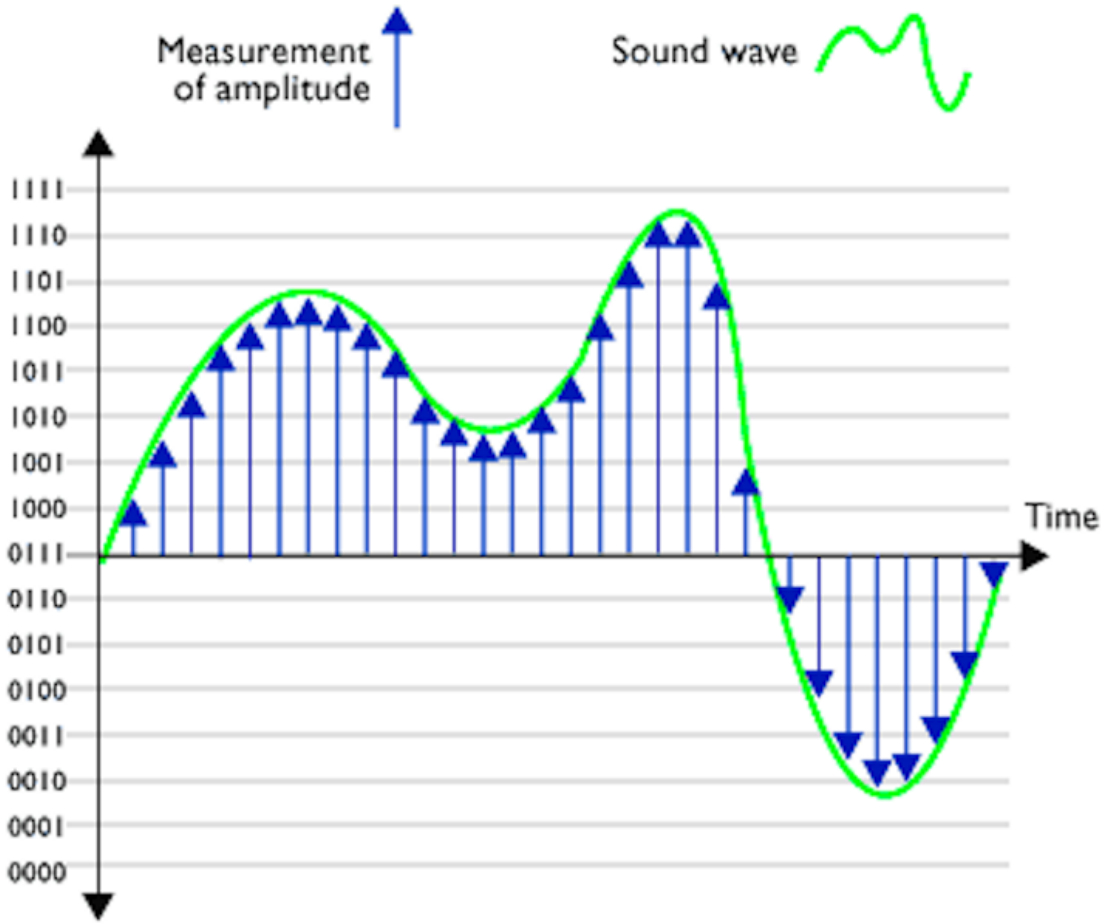
Outline

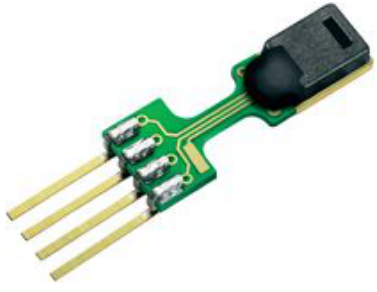
Introduction to Analog to Digital Converters (1/2)

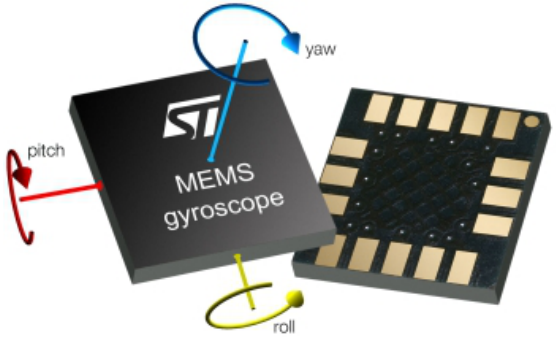
Definition

An analog-to-digital converter is a device that converts a continuous quantity to a discrete time digital representation

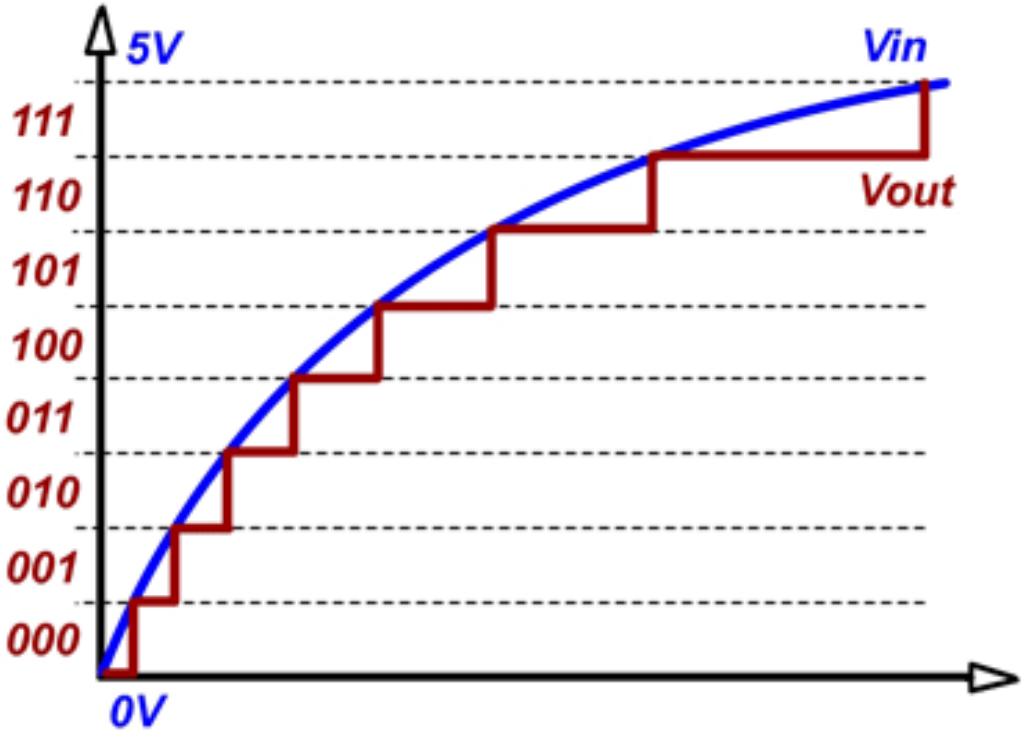


Introduction to Analog to Digital Converters (2/2)





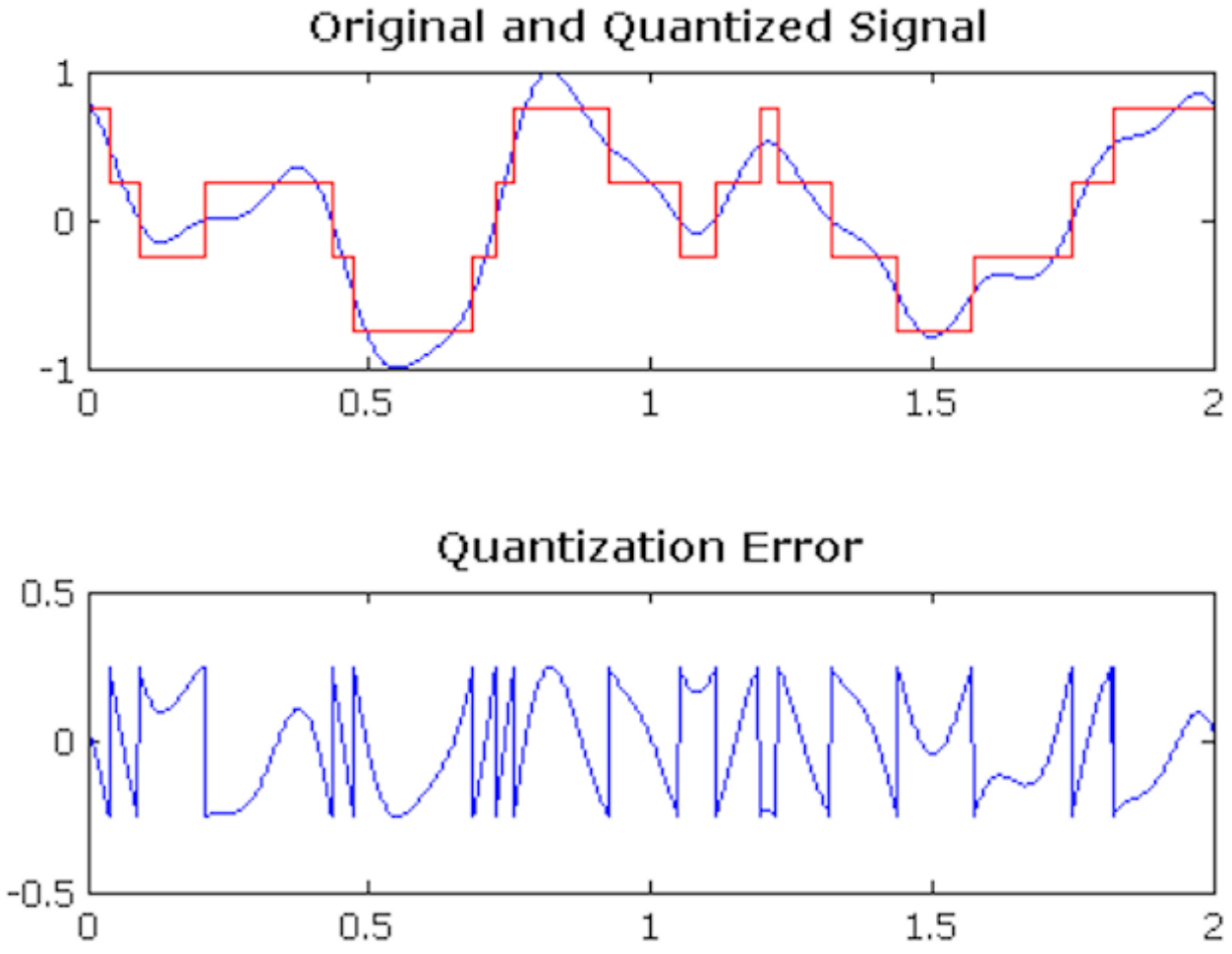
Continuous quantity to discrete quantity (1/2)



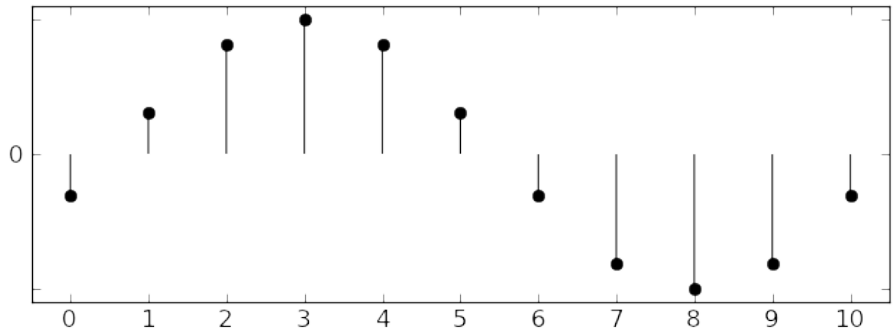
$$N = 2^n$$

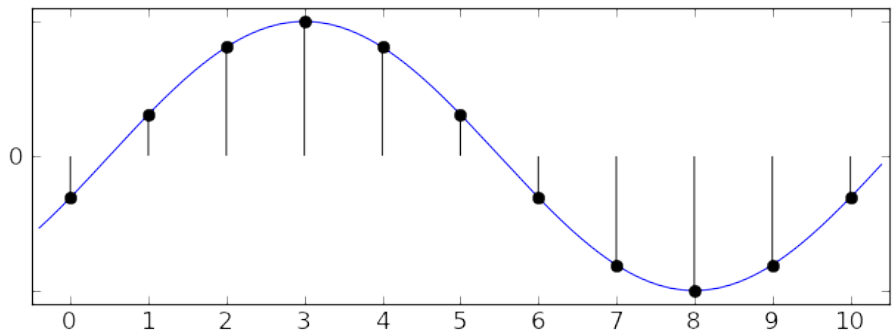
$$LSB = V_{REF}/2^n$$

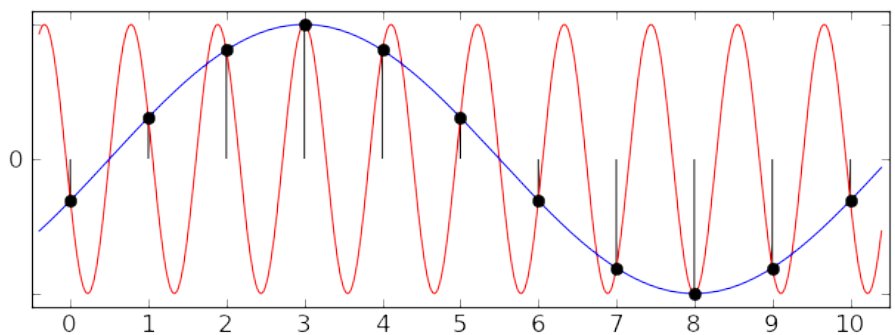
Continuous quantity to discrete quantity (2/2)



Continuous time to discrete time (1/2)







Continuous time to discrete time (2/2)

Nyquist rate

The Nyquist rate is the minimum sampling rate required to avoid aliasing, equal to twice the highest frequency contained within the signal.

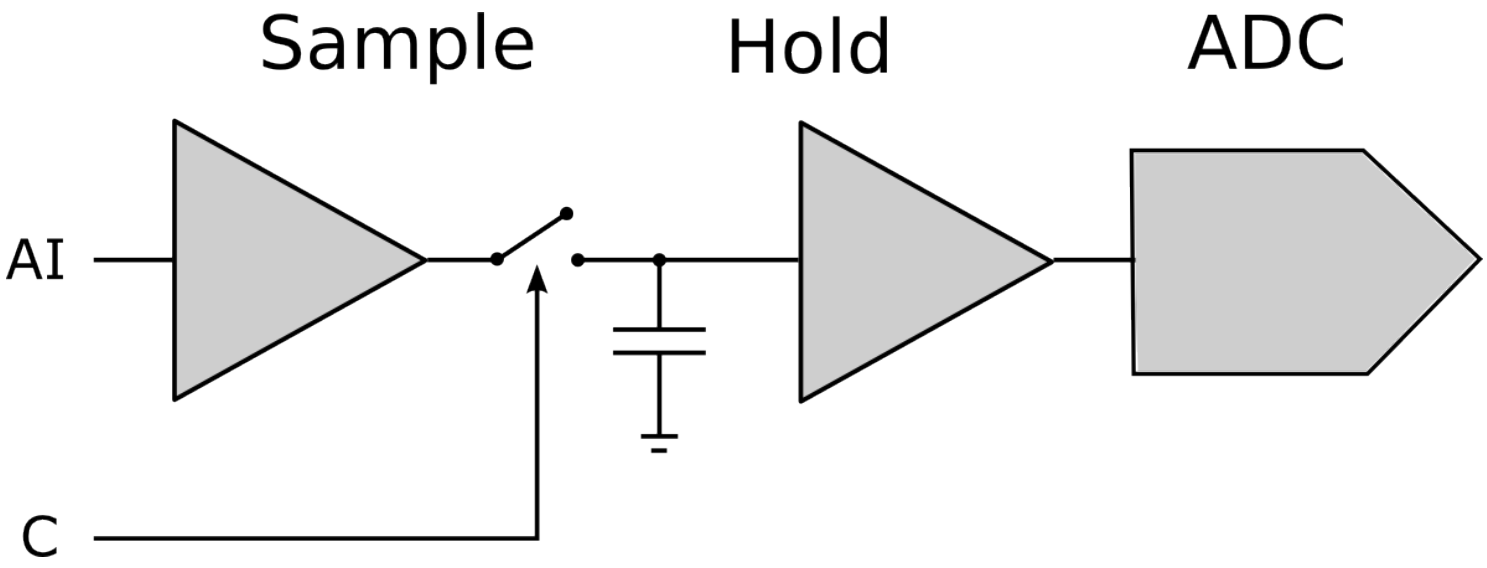
$$f_N \stackrel{\text{def}}{=} 2B$$

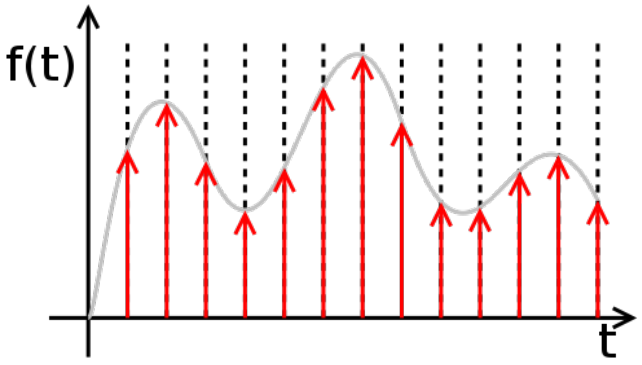
Minimum sampling rate

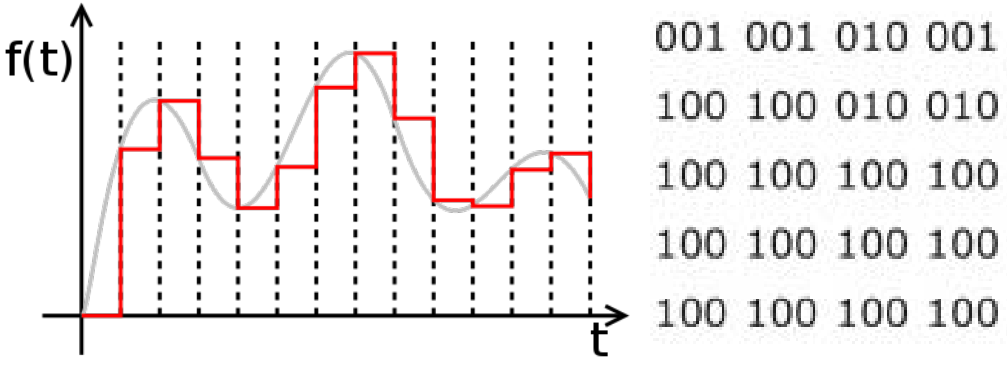
To avoid aliasing, the sampling rate must exceed the Nyquist rate.

$$f_S > f_N$$

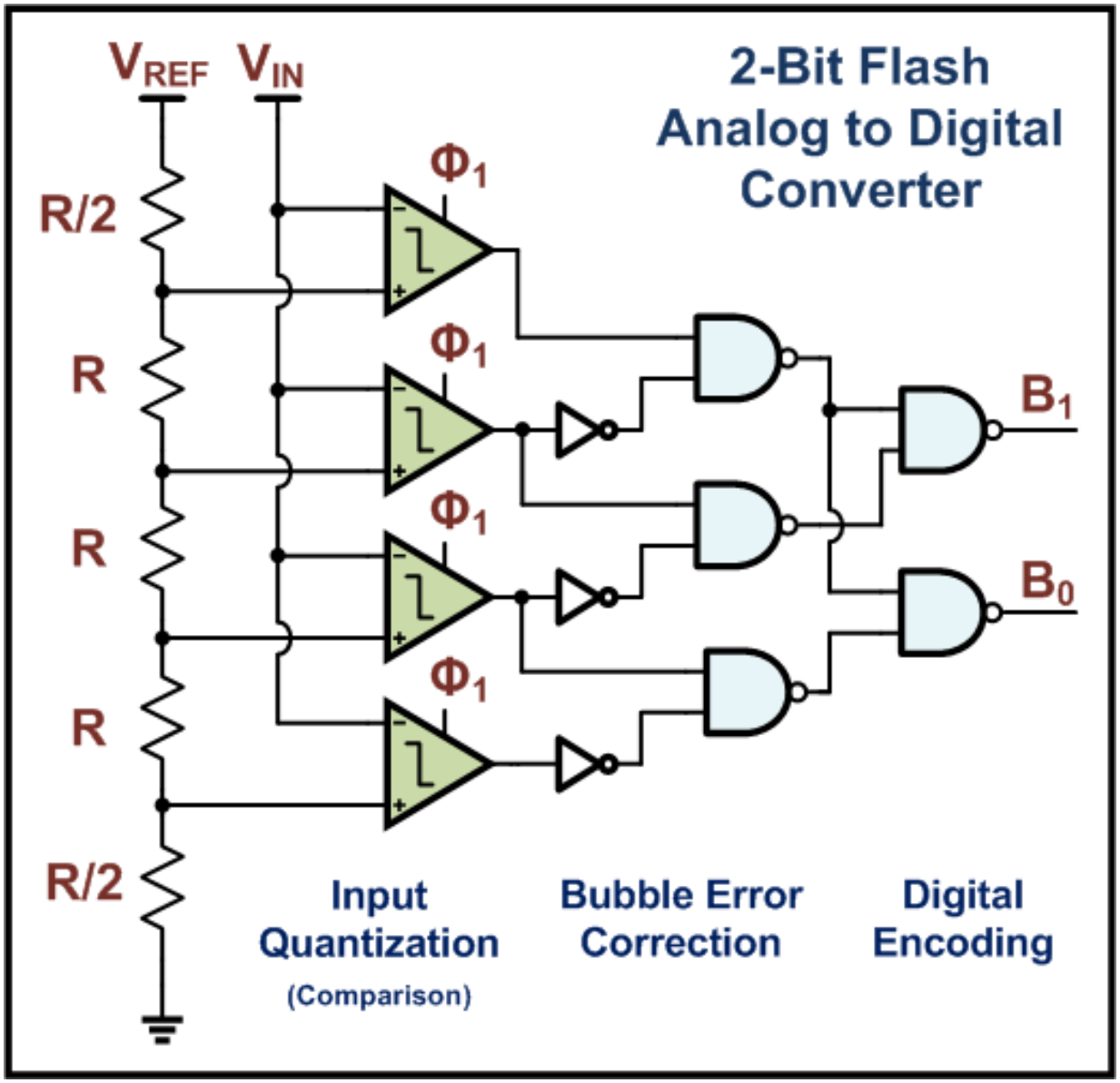
Analog to Digital Converter diagram



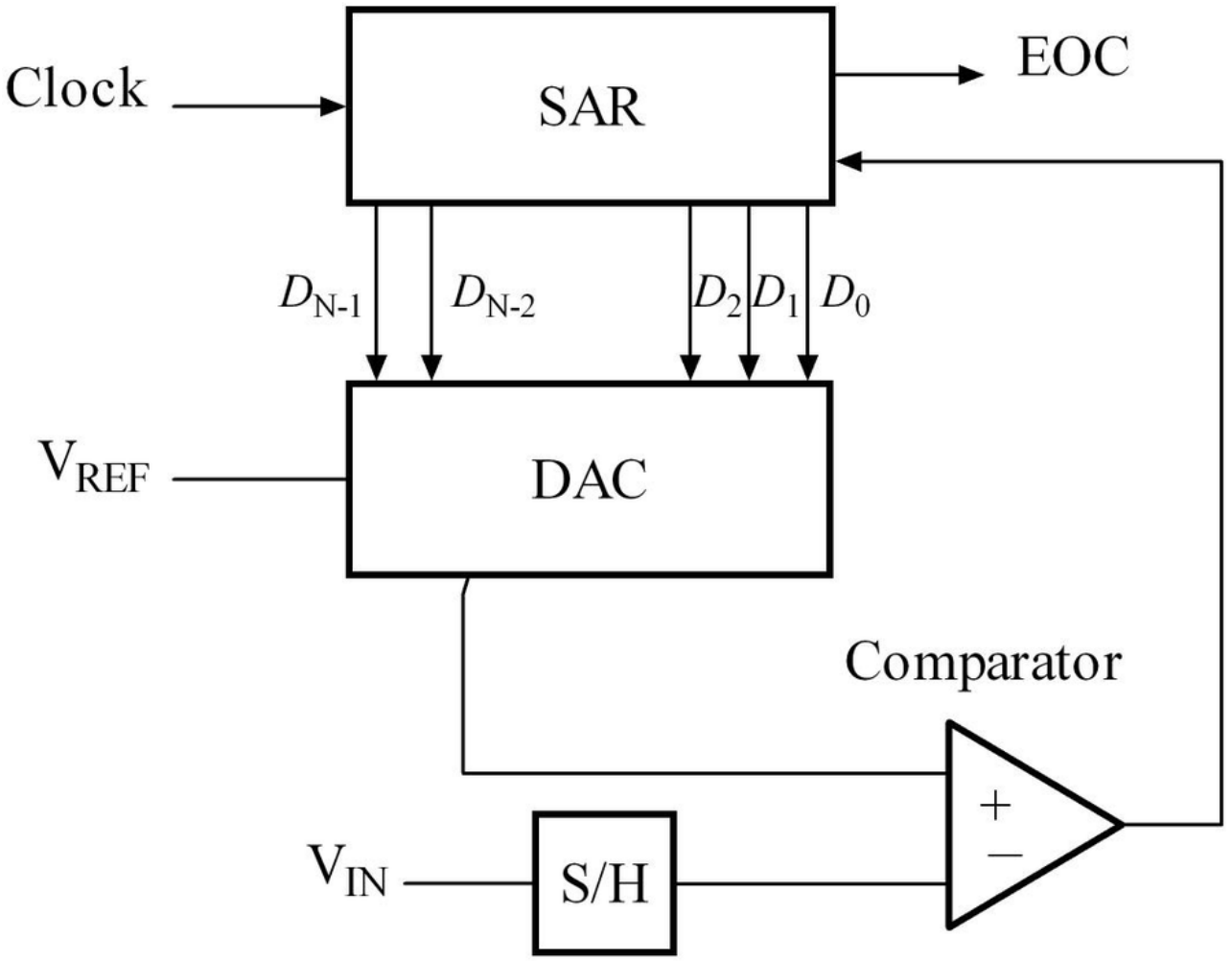




FLASH Analog to Digital Converter



SAR Analog to Digital Converter



Sigma-delta Analog to Digital Converter

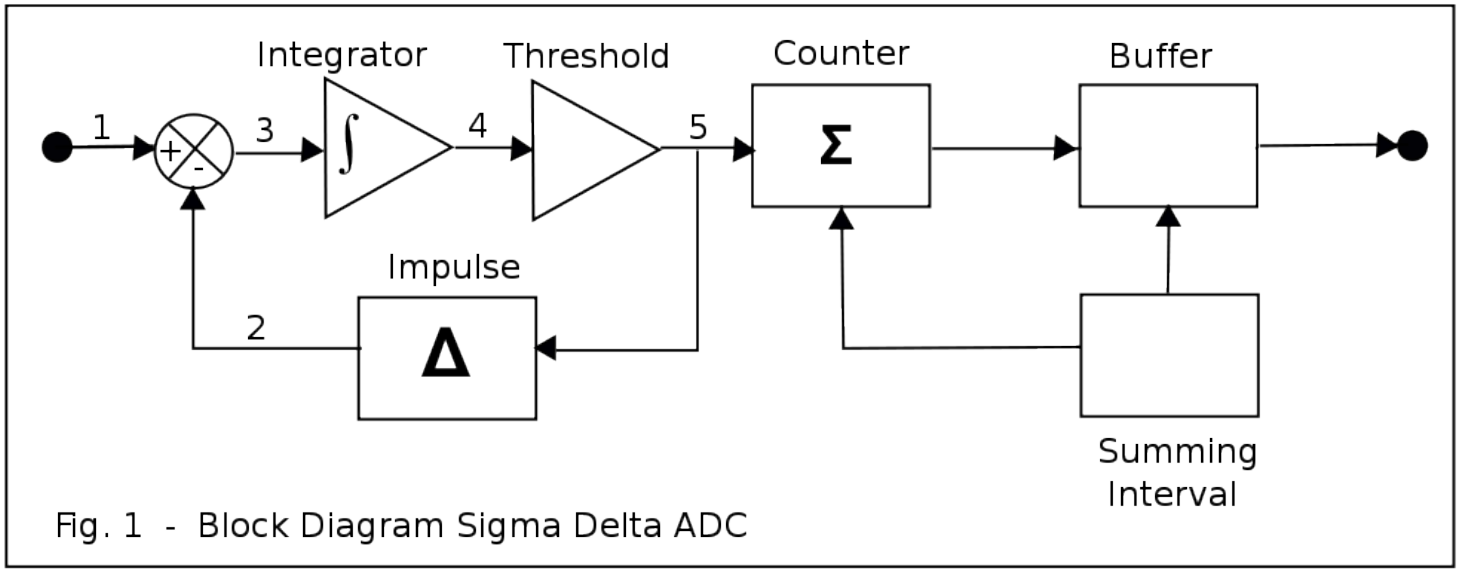
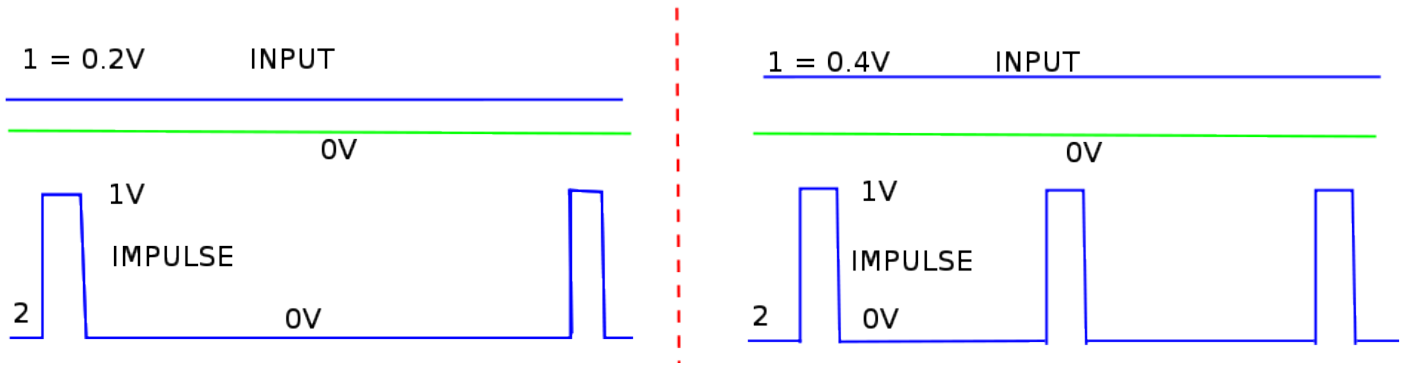


Fig. 1 - Block Diagram Sigma Delta ADC

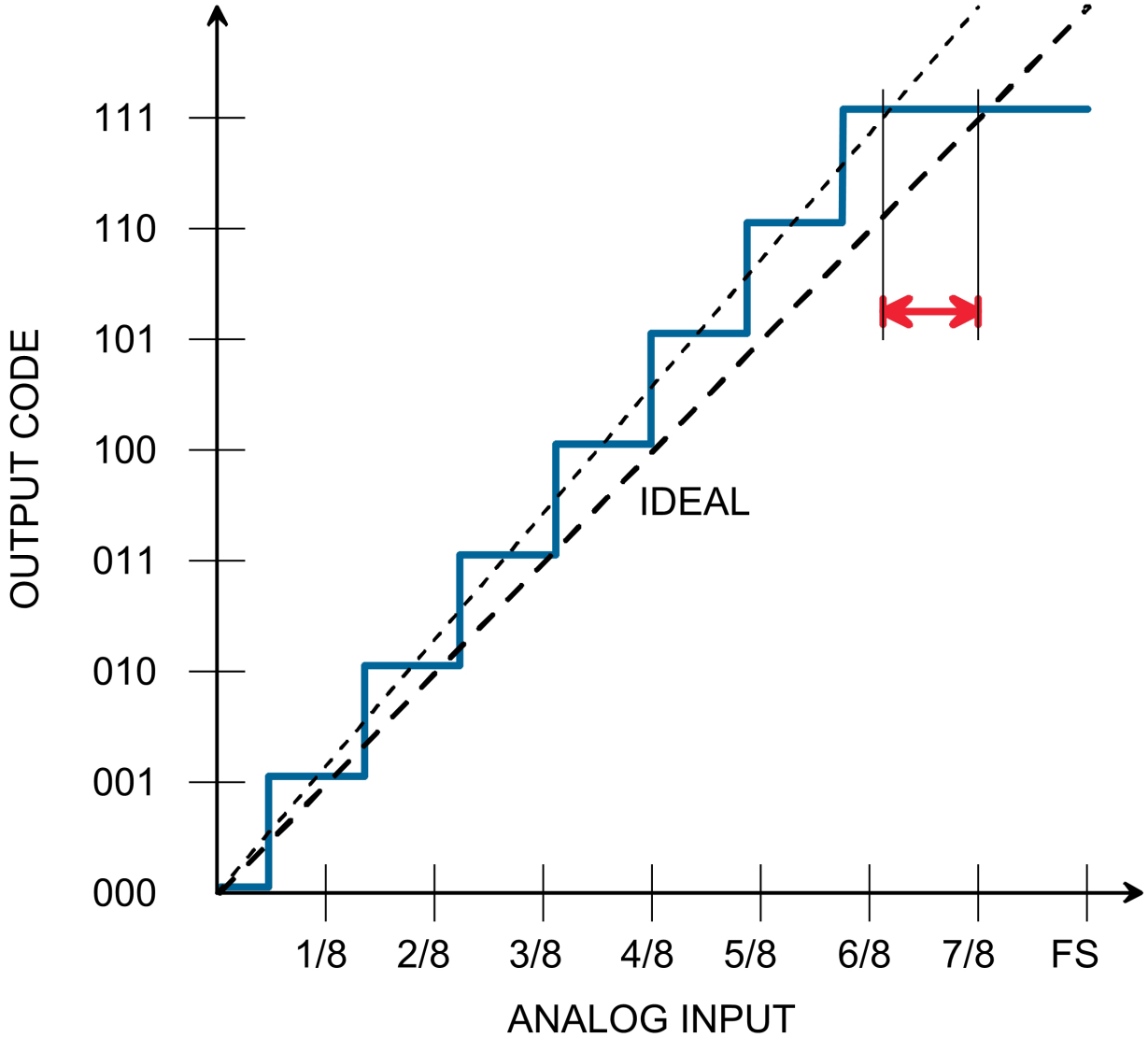


Analog to Digital Converter characteristics

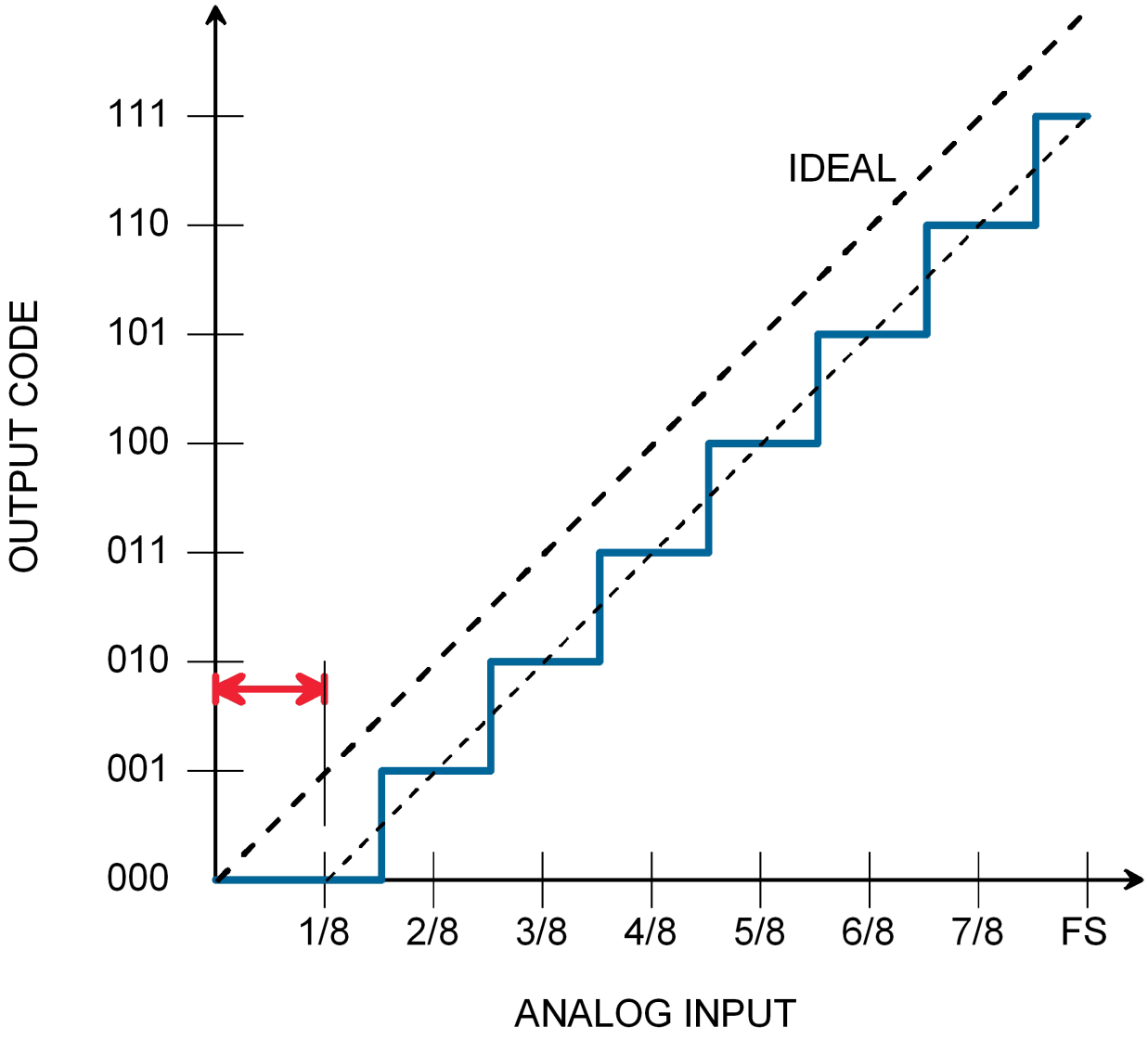
- Resolution
- Max sampling rate
- Signal to Noise Ratio (SNR)
- Input voltage offset
- Gain stability
- Linearity

ANALOG INPUT	
Standard Differential Input Range	
Single-Ended Input Voltage	
Common-Mode Voltage	
Optional Input Ranges	
Analog Input Bias Current	
Track-Mode Input Bandwidth	
Input Impedance	
CONVERSION CHARACTERISTICS	
Sample Rate	
Data Latency	
DYNAMIC CHARACTERISTICS	
Differential Linearity Error (largest code error)	
f = 1MHz	
f = 10MHz	
No Missing Codes	
Integral Nonlinearity Error, f = 1MHz	
Spurious-Free Dynamic Range(1)	
f = 1MHz	
f = 10MHz	
f = 31MHz	
2-Tone Intermodulation Distortion	
f_{IN} = 19.4MHz and 20.4MHz (–7dB each tone)	
Signal-to-Noise Ratio (SNR)	
f = 1MHz	
f = 10MHz	
f = 31MHz	
Signal-to-(Noise + Distortion) (SINAD)	
f = 1MHz	
f = 10MHz	
f = 31MHz	

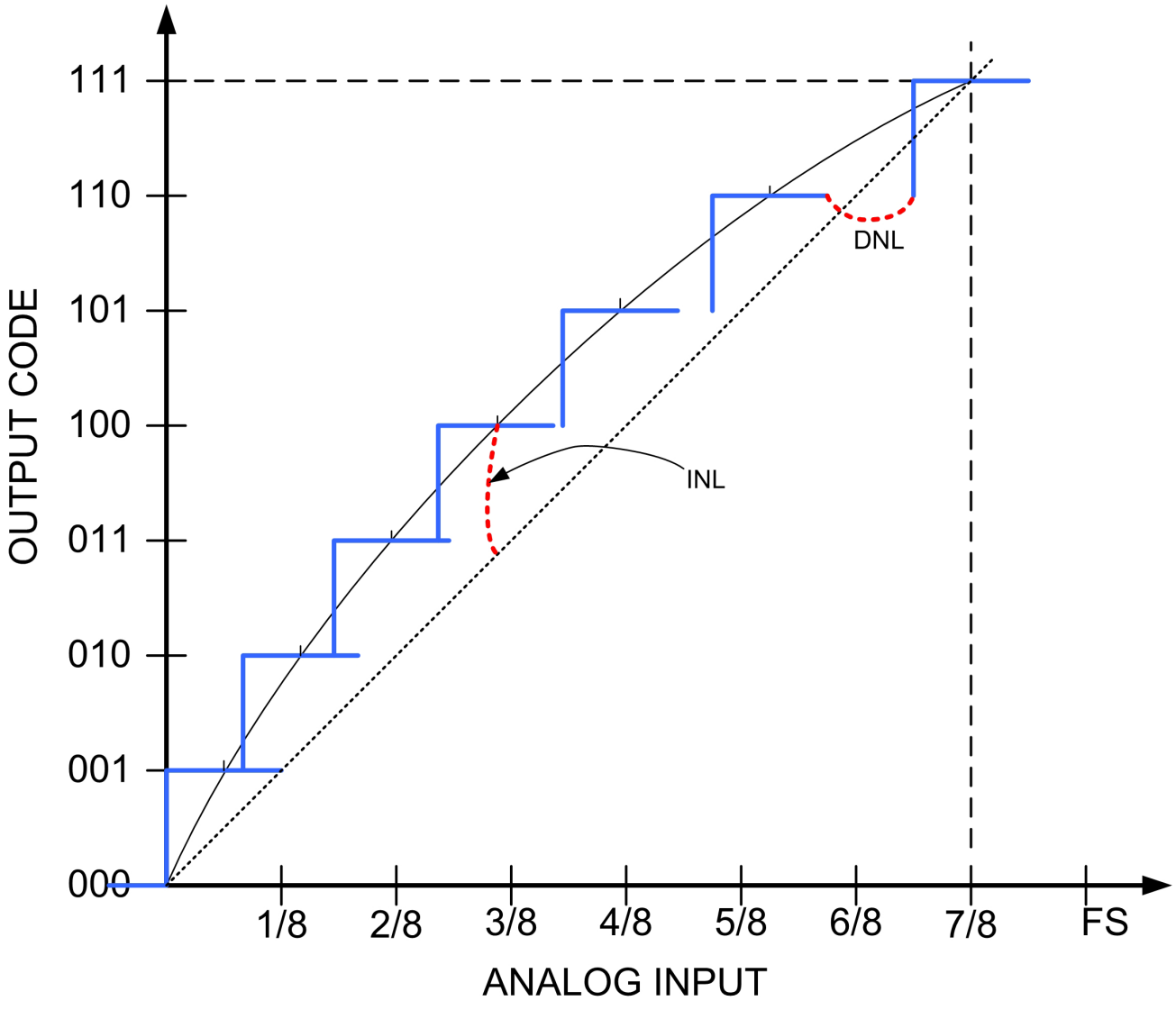
Gain error


111
110
101
100
011
010
001
000
OUTPUT CODE
IDEAL
1/8
2/8
3/8
4/8
5/8
6/8
7/8
FS
ANALOG INPUT

Voltage offset error



Non-linearity errors

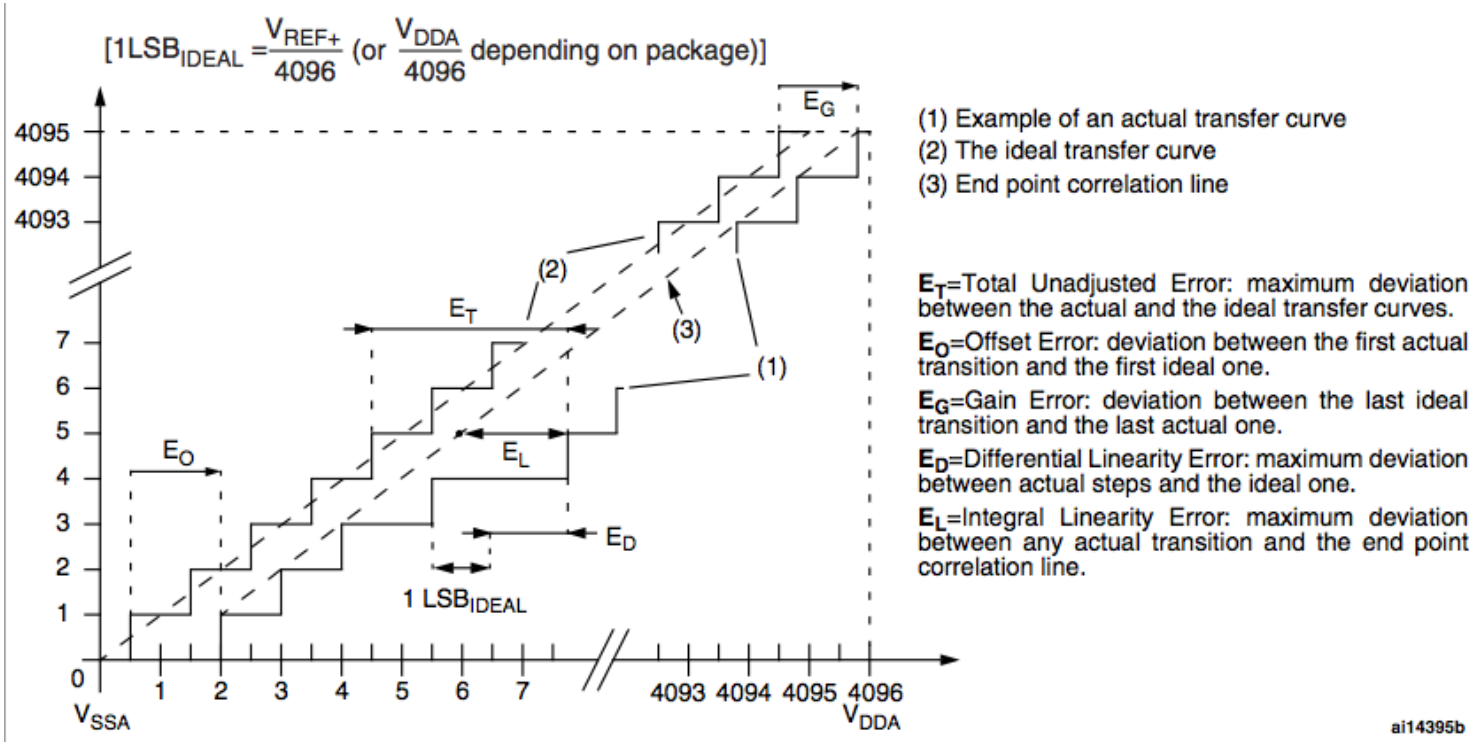


Outline

STM32 Analog do Digital Converter

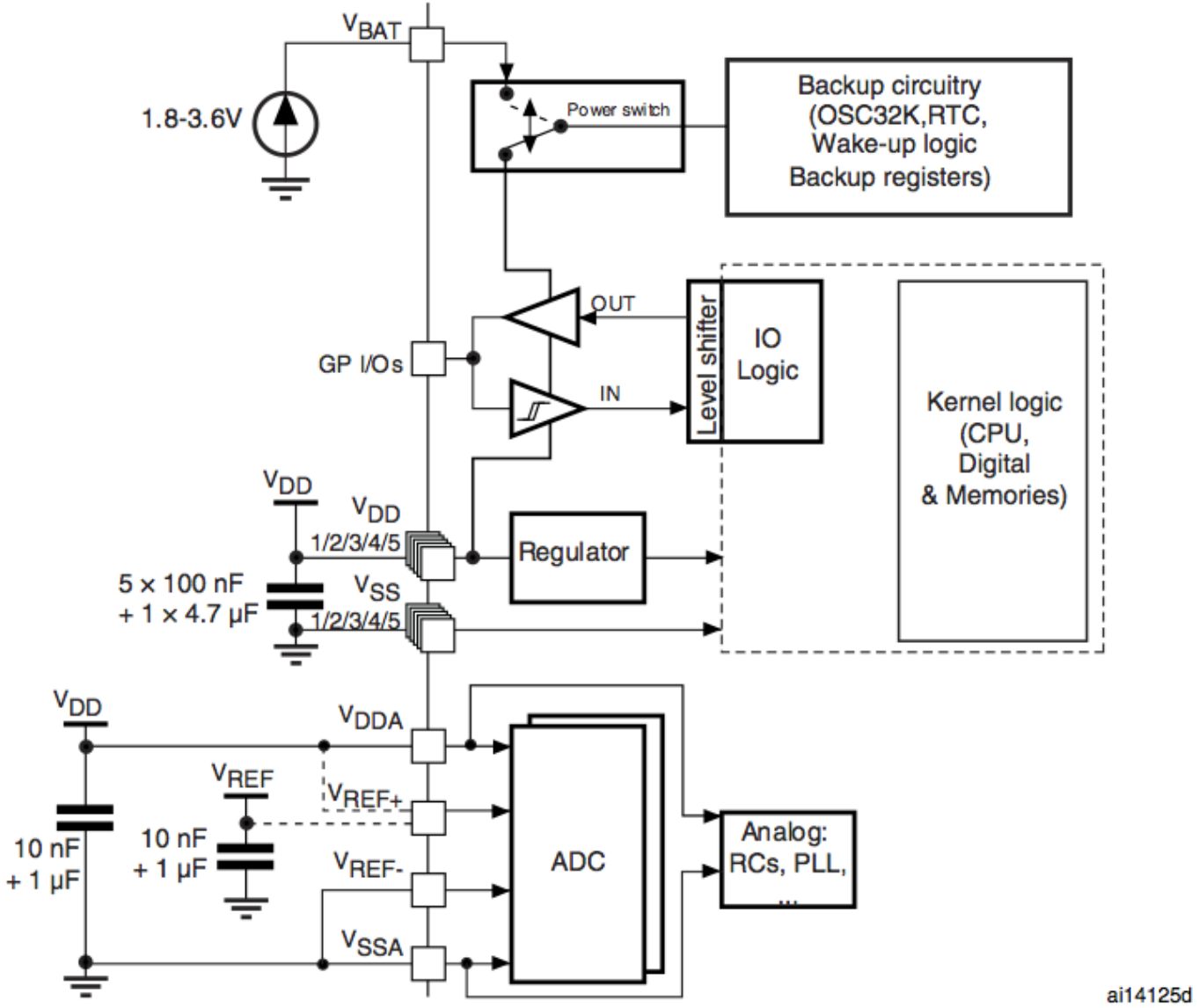
- Successive approximation analog-to-digital converter
- 12-bit resolution
- Interrupt generation at End of Conversion, End of Injected conversion and Analog watchdog event
- Single and continuous conversion modes
- Scan mode for automatic conversion of channel 0 to channel n
- Self-calibration
- External trigger option for both regular and injected conversion
- Total conversion time: 14 to 252 T_{CK} (t_S for sampling + 12.5 for successive approximation)

STM32 Analog do Digital Converter accuracy

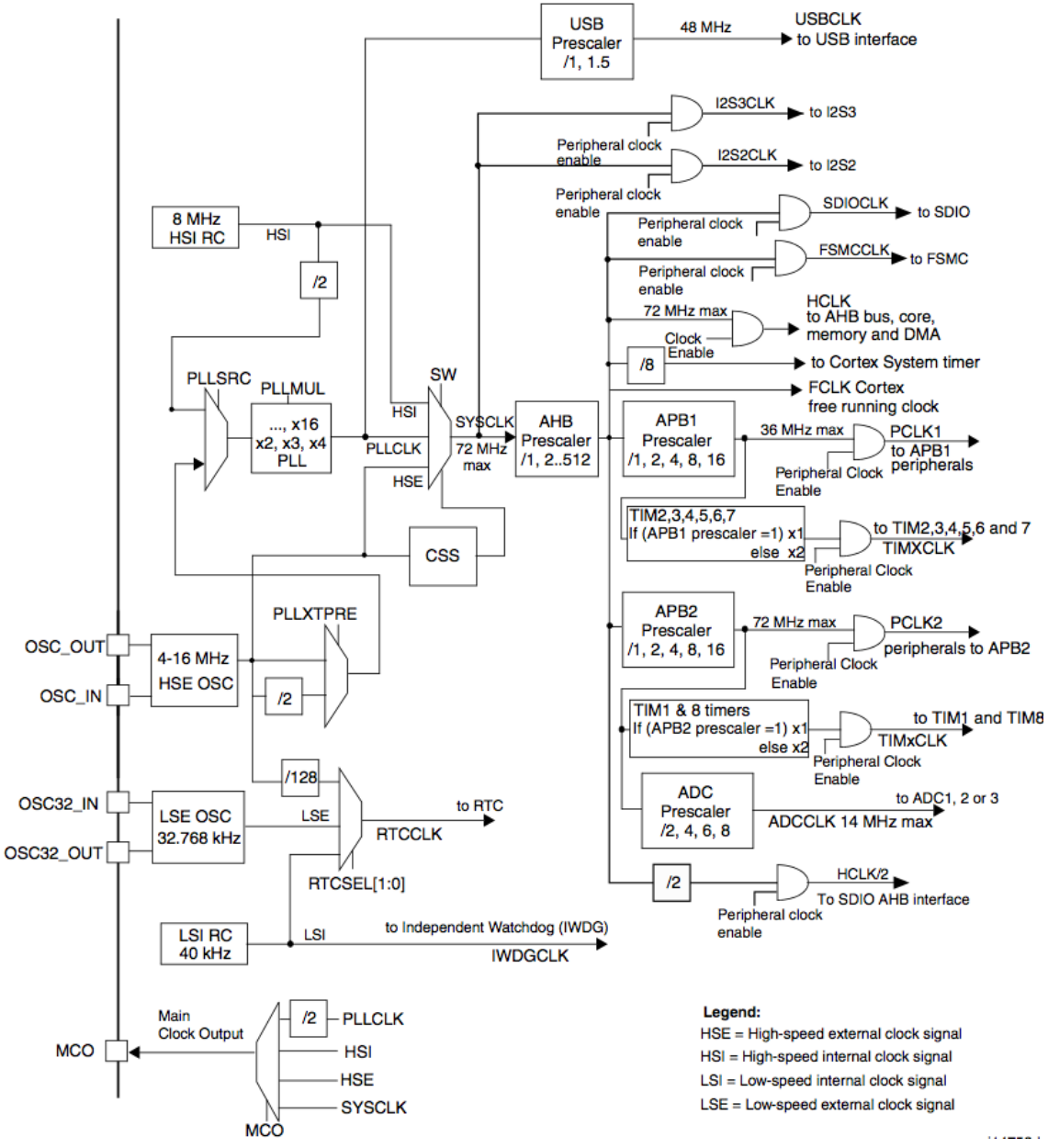


Symbol	Parameter	Test conditions	Typ	Max(4)	Unit
ET	Total unadjusted error	f_{PCLK2} = 56 MHz, f_{ADC} = 14 MHz, R_{AIN} < 10 kΩ, V_{DDA} = 2.4 V to 3.6 V Measurements made after ADC calibration	±2	±5	LSB
EO	Offset error		±1.5	±2.5	
EG	Gain error		±1.5	±3	
ED	Differential linearity error		±1	±2	
EL	Integral linearity error		±1.5	±3	

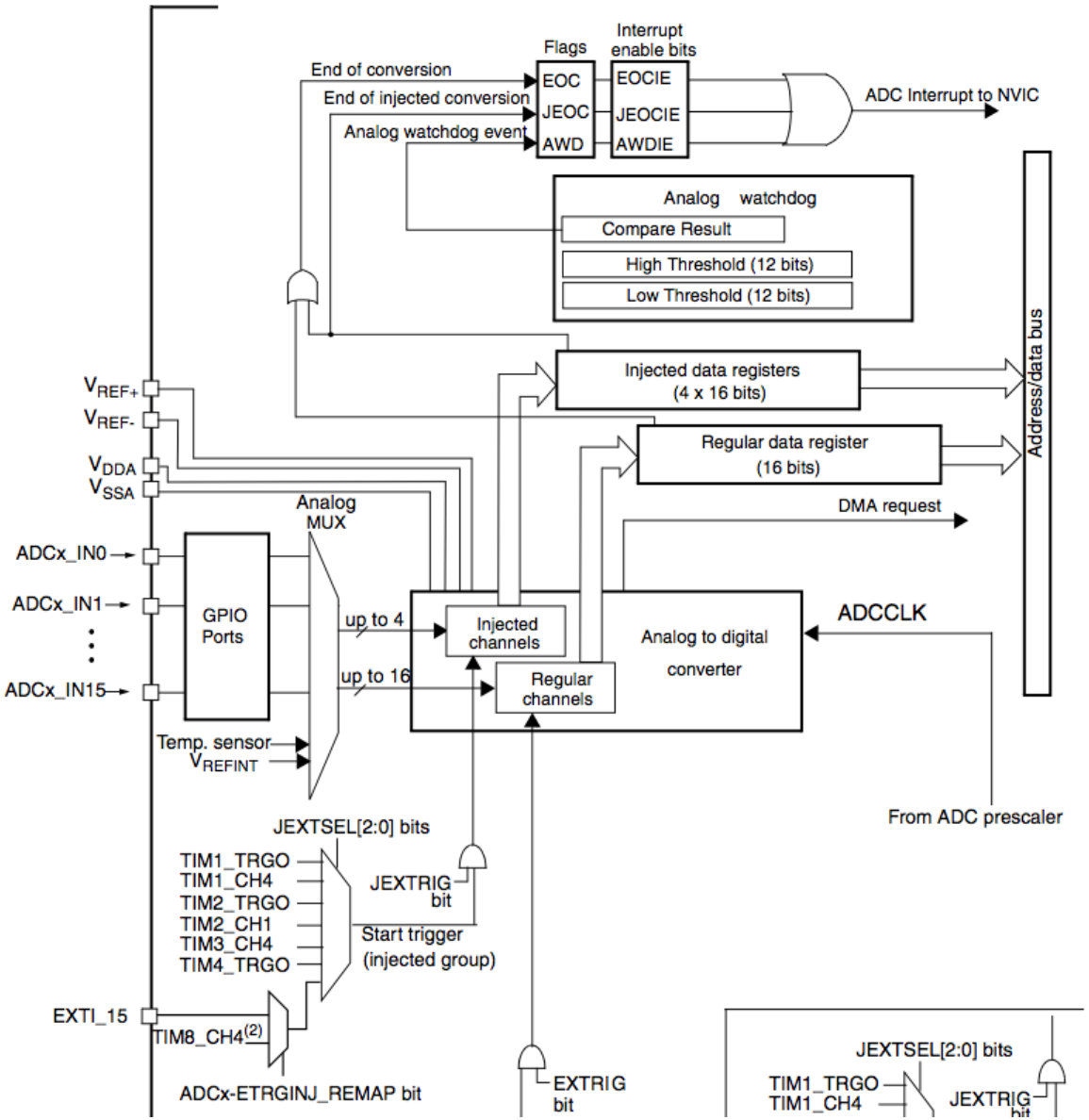
Analog power supply



STM32 clock tree



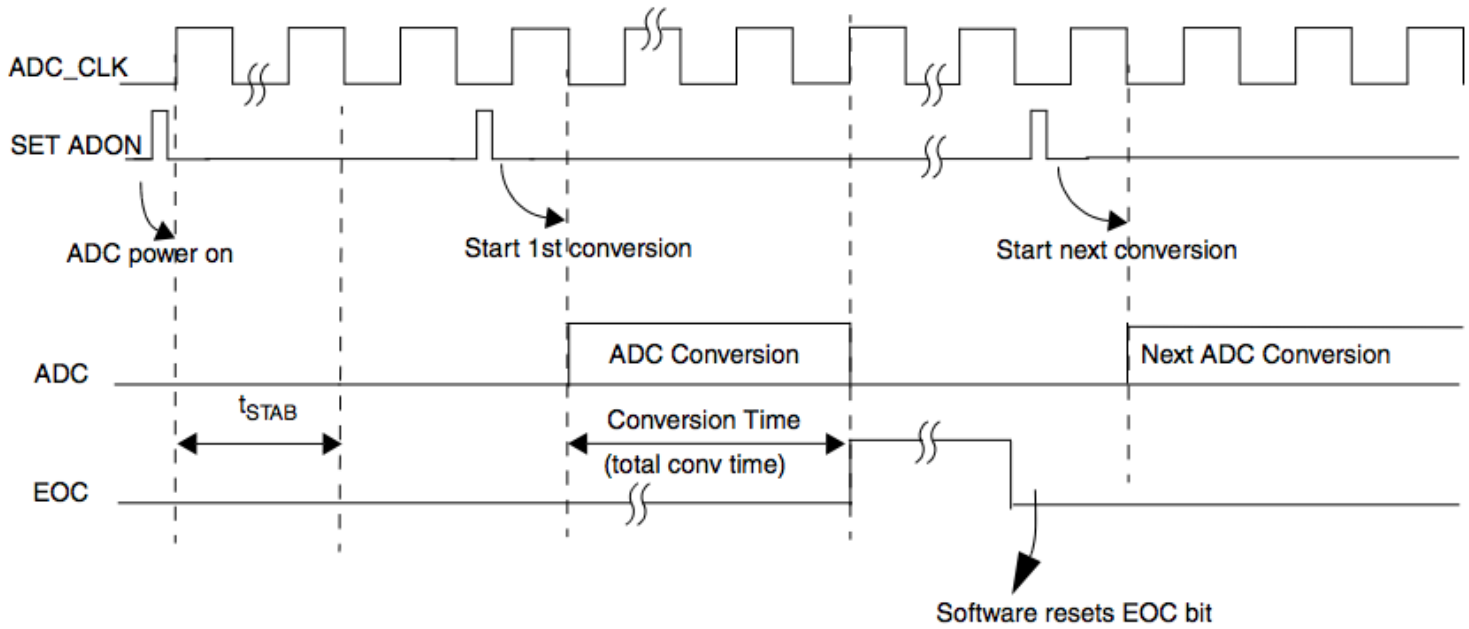
STM32 Analog do Digital Converter diagram



Channel selection

- 16 multiplexed channels
- It is possible to organize the conversions in groups
- A group consists of a sequence of conversions which can be done on any channel and in any order
- Regular group:
  - up to 16 conversions
  - the conversion sequence must be selected in the ADC_SQRx registers
- Injected group:
  - up to 4 conversions
  - This mode is intended for use when conversion is triggered by an external event or by software
  - The injected group has priority over the regular channel group
  - It interrupts the conversion of the current channel in the regular channel group

Single and continuous conversion mode

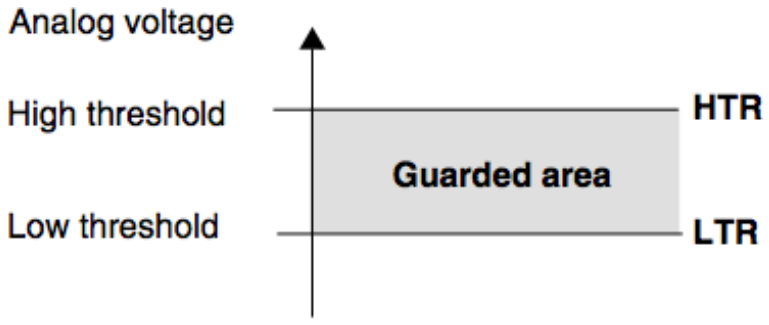


- In Single conversion mode the ADC does one conversion
- In Continuous mode (CONT = 1) another conversion starts as soon as it finishes one
- The conversion is started either by setting the ADON bit or by external trigger
- If the EOCIE is set, an interrupt is generated at the end of each conversion

Scan conversion mode

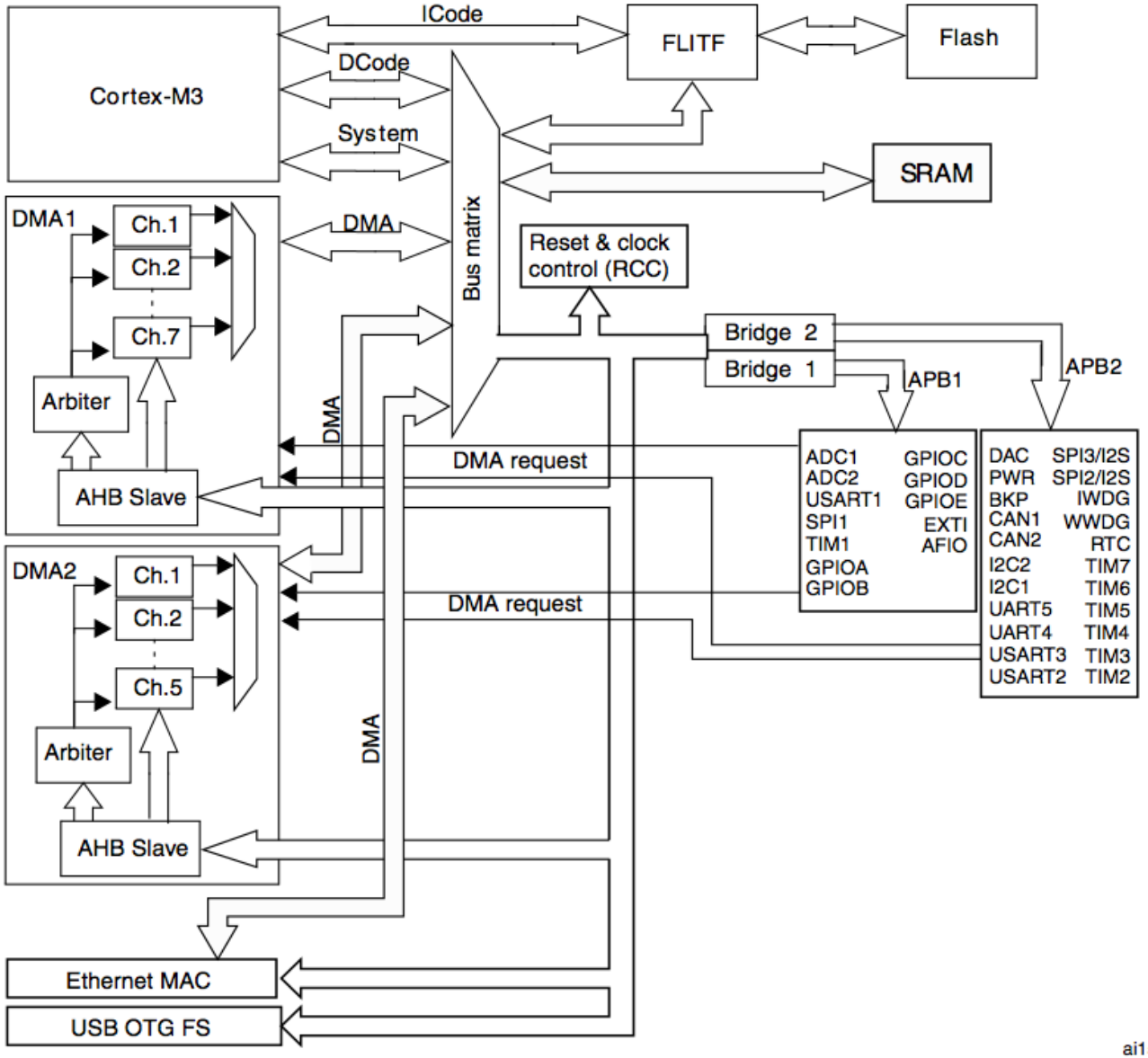
- Scans a group of analog channels
- A single conversion is performed for each channel of the group
- After each end of conversion the next channel of the group is converted automatically
- If CONT = 1, on last channel conversion, the ADC starts again from the first group channel
- If the DMA bit is set, the direct memory access controller is used to transfer the converted data to SRAM after each EOC

Analog watchdog



- The AWD analog watchdog status bit is set if the analog voltage converted by the ADC is below a low threshold or above a high threshold
- These thresholds are programmed in the 12 least significant bits of the ADC_HTR and ADC_LTR 16-bit registers
- An interrupt can be enabled by using the AWDIE bit in the ADC_CR1 register

Direct Memory Access



ADC and DMA

- Converted regular channels value are stored in a unique data register
- It is necessary to use DMA for conversion of more than one regular channel
- The end of conversion of a regular channel generates a DMA request
- Converted data is transferred from the ADC_DR register to the destination location selected by the user

Outline

ADC status register (ADC_SR)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved											STRT	JSTRT	JEOC	EOC	AWD
Res.											rc_w0	rc_w0	rc_w0	rc_w0	rc_w0

0 **AWD**: Analog watchdog flag
This bit is set by hardware when the converted voltage crosses the values programmed in the ADC_LTR and ADC_HTR registers. It is cleared by software.
0: No Analog watchdog event occurred
1: Analog watchdog event occurred

1 **EOC**: End of conversion
This bit is set by hardware at the end of a group channel conversion (regular or injected). It is cleared by software or by reading the ADC_DR.
0: Conversion is not complete
1: Conversion complete

4 **STRT**: Regular channel start flag
This bit is set by hardware when regular channel conversion starts. It is cleared by software.
0: No regular channel conversion started
1: Regular channel conversion has started

ADC control register 1 (ADC_CR1)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved								AWDEN	JAWDEN	Reserved		DUALMOD[3:0]			
Res.								rw	rw	Res.		rw	rw	rw	rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DISCNUM[2:0]			JDISCEN	DISCEN	JAUTO	AWDSGL	SCAN	JEOC IE	AWDIE	EOCIE	AWDCH[4:0]				
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

4:0 **AWDCH[4:0]**: Analog watchdog channel select bits
These bits are set and cleared by software. They select the input channel to be guarded by the Analog watchdog.
00000: ADC analog input Channel0
...
10001: ADC analog input Channel17

5 **EOCIE**: Interrupt enable for EOC
This bit is set and cleared by software to enable/disable the End of Conversion interrupt.
0: EOC interrupt disabled
1: EOC interrupt enabled. An interrupt is generated when the EOC bit is set.

8 **SCAN**: Scan mode
This bit is set and cleared by software to enable/disable Scan mode. In Scan mode, the inputs selected through the ADC_SQRx or ADC_JSQRx registers are converted.
0: Scan mode disabled
1: Scan mode enabled

ADC control register 2 (ADC_CR2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved								TSVREFE	SWSTART	JSWSTART	EXTTRIG	EXTSEL[2:0]			Res.
Res.								rw	rw	rw	rw	rw	rw	rw	

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
JEXTTRIG	JEXTSEL[2:0]			ALIGN	Reserved		DMA	Reserved				RSTCAL	CAL	CONT	ADON
rw	rw	rw	rw	rw	Res.		rw	Res.				rw	rw	rw	rw

0 **ADON**: A/D converter ON/OFF
If this bit holds a value of zero and a 1 is written to it then it wakes up the ADC from Power Down state.
Conversion starts when this bit holds a value of 1 and a 1 is written to it.
0: Disable ADC conversion and go to power down mode.
1: Enable ADC and to start conversion

1 **CONT**: Continuous conversion
0: Single conversion mode
1: Continuous conversion mode

8 **DMA**: Direct memory access mode
0: DMA mode disabled
1: DMA mode enabled

11 **ALIGN**: Data alignment
0: Right Alignment
1: Left Alignment

ADC sample time register 1 (ADC_SMPR1)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved								SMP17[2:0]			SMP16[2:0]			SMP15[2:1]	
Res.								rw	rw	rw	rw	rw	rw	rw	rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SMP 15_0	SMP14[2:0]			SMP13[2:0]			SMP12[2:0]			SMP11[2:0]			SMP10[2:0]		
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

4:0 **SMPx[2:0]**: Channel x Sample time selection
These bits are written by software to select the sample time individually for each channel.
000: 1.5 cycles
001: 7.5 cycles
010: 13.5 cycles
011: 28.5 cycles
100: 41.5 cycles
101: 55.5 cycles
110: 71.5 cycles
111: 239.5 cycles

ADC regular sequence register 1 (ADC_SQR1)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved								L[3:0]				SQ16[4:1]			
Res.								rw	rw	rw	rw	rw	rw	rw	rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SQ16_0	SQ15[4:0]					SQ14[4:0]					SQ13[4:0]				
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

19:15 **SQ16[4:0]**: 16th conversion in regular sequence
These bits are written by software with the channel number (0..17) assigned as the 16th in the conversion sequence.

23:20 **L[3:0]**: Regular channel sequence length
These bits are written by software to define the total number of conversions in the regular channel conversion sequence.
0000: 1 conversion
0001: 2 conversions
...
1111: 16 conversions

ADC *value* registers

- ADC regular data register (ADC_DR)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADC2DATA[15:0]															
r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA[15:0]															
r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r

- ADC watchdog low threshold register (ADC_LTR)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved				LT[11:0]											
Res				rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

- ADC watchdog low threshold register (ADC_HTR)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved				HT[11:0]											
				rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

References

http://en.wikipedia.org/wiki/Analog_to_digital_converter

http://en.wikipedia.org/wiki/Sample_and_hold

http://en.wikipedia.org/wiki/Quantization_error

http://en.wikipedia.org/wiki/Nyquist_rate

http://en.wikipedia.org/wiki/Nyquist_frequency

http://en.wikipedia.org/wiki/Flash_ADC

http://en.wikipedia.org/wiki/Successive_Approximation_ADC

http://en.wikipedia.org/wiki/Sigma-delta_modulation

STM32F10xxx Reference Manual (RM0008 - Doc ID 14611)

Application note: STM32 ADC modes and their applications (AN3116 - Doc ID 16840)