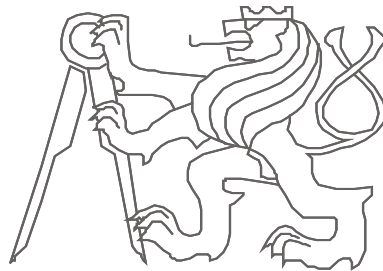


# Architektury počítačů

## MZ-APO a I/O operace

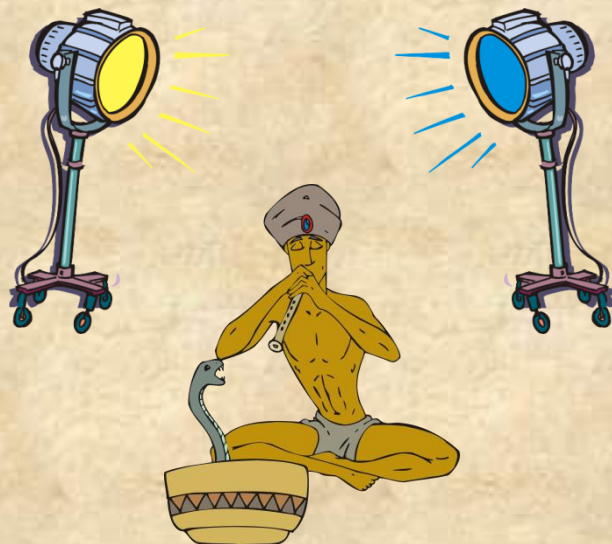


České vysoké učení technické, Fakulta elektrotechnická

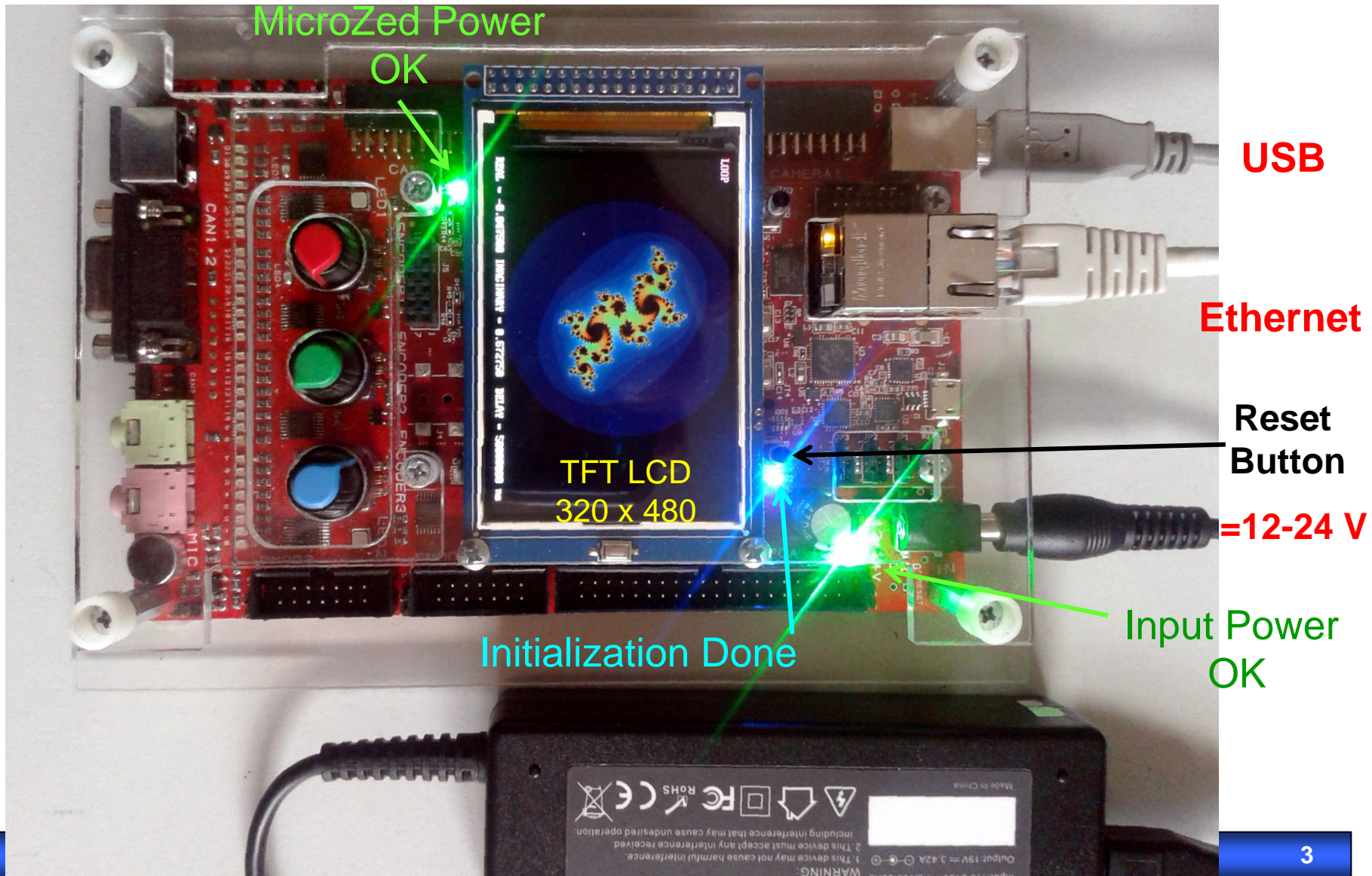
# *Zadání úlohy*

Naprogramujte řídicí jednotku MicroZed na ovládací prvek dvou RGB reflektorů.

Volba odstínu barvy světla se zadává v barevném modelu HSV/HSB.



# MZAPO - MicroZed\_APO board



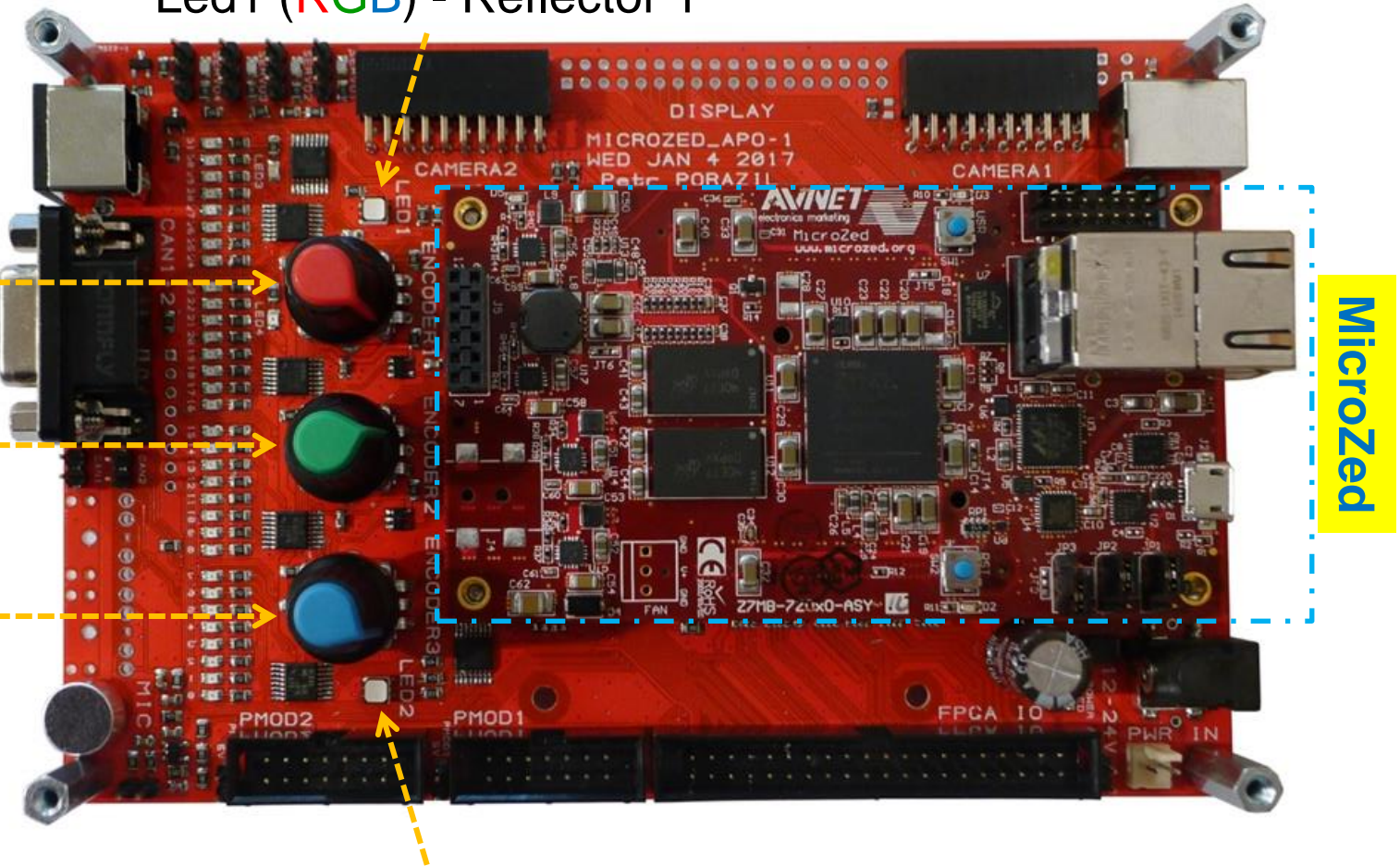
# Demounting LCD -> MicroZed\_APO on Carry card

Led1 (RGB) - Reflector 1

Red Knob

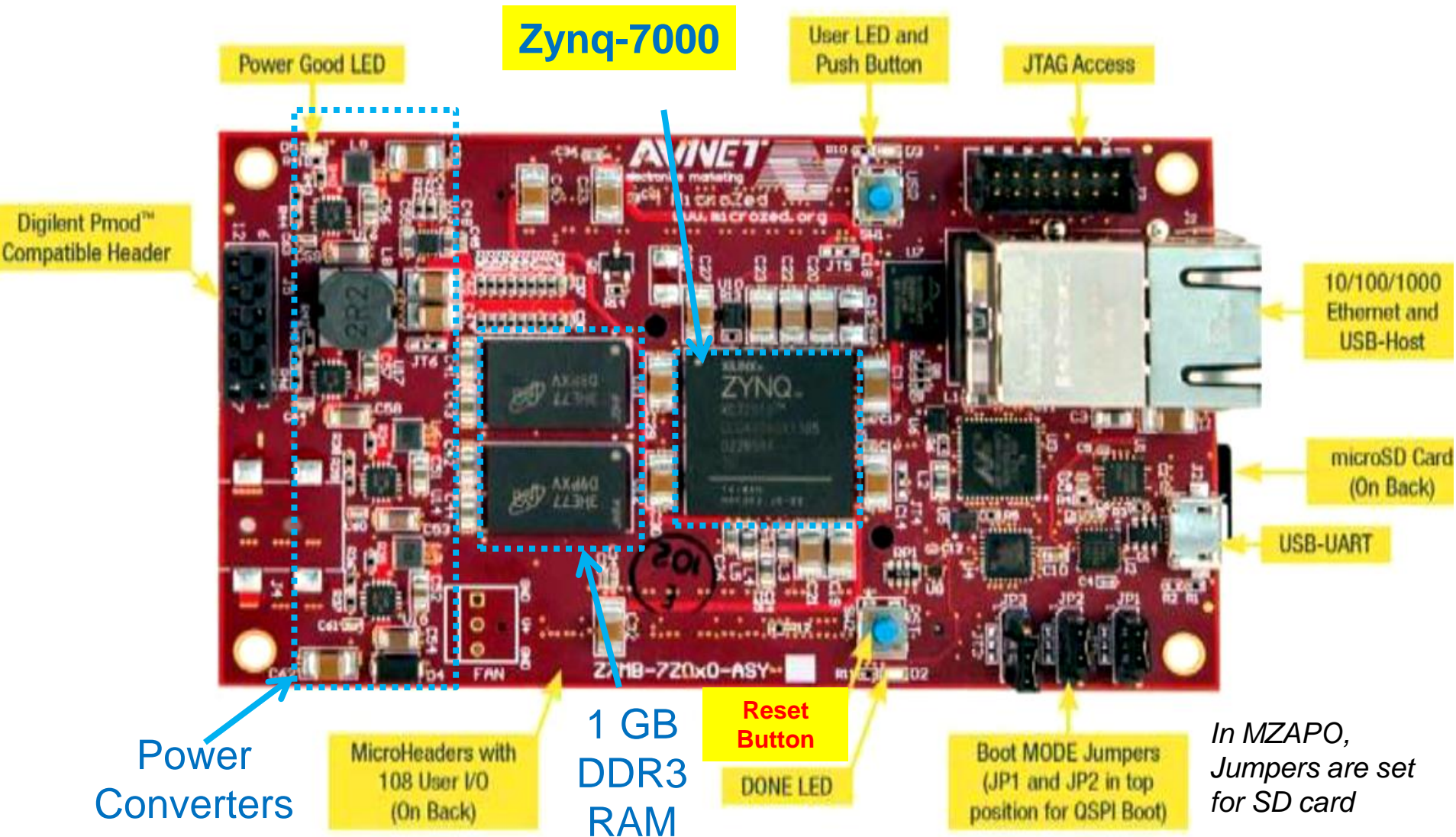
Green Knob

Blue Knob



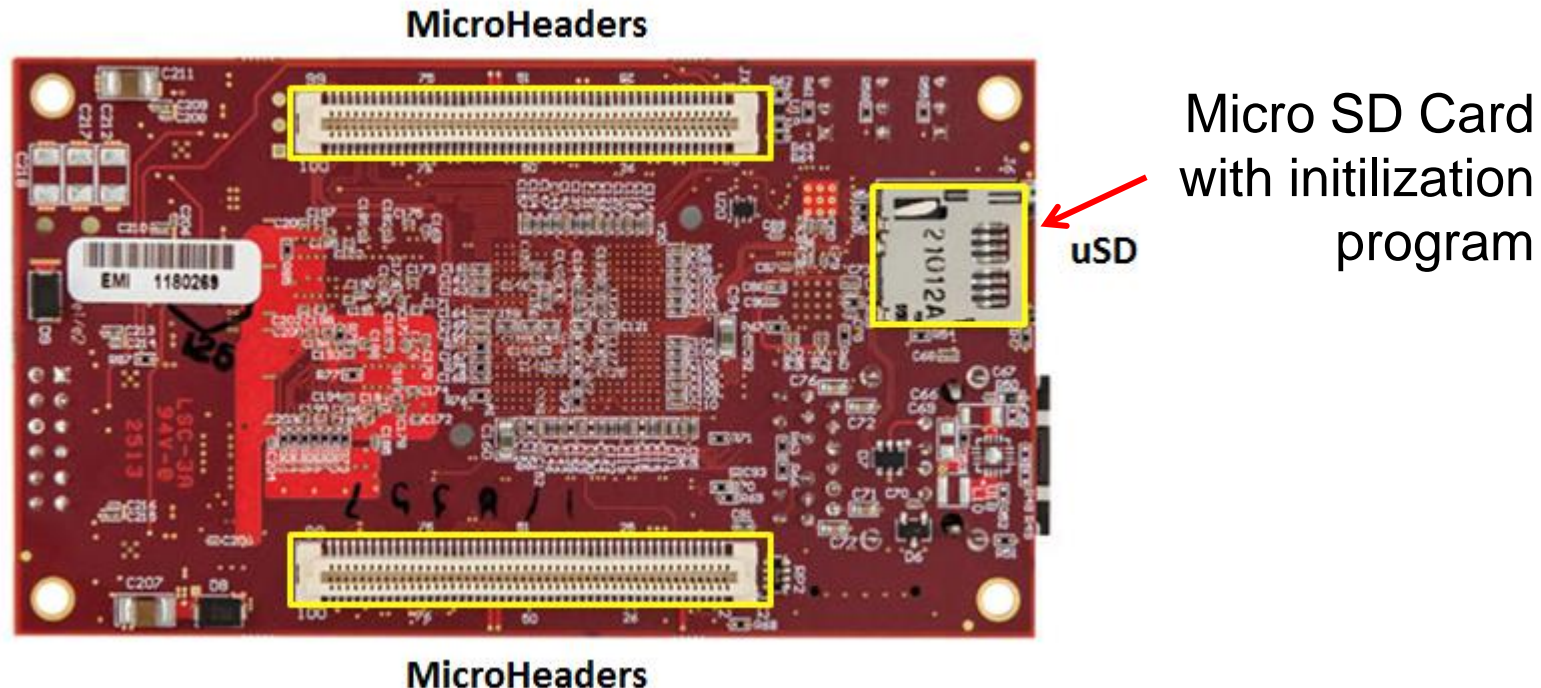
Led2 (RGB) - Reflector2

# MicroZed - Top View



## MicroZed - Bottom View

### Microzed Evaluation Kit - ADSAES-Z7MB-7Z010-G



108-pin micro header connectors allowing mount MicroZed™ Evaluation Kit to a carrier card.

*Price of 1 pcs of used Zynq: ~ \$45 , price of MicroZed: ~ \$180 (April 2019)*

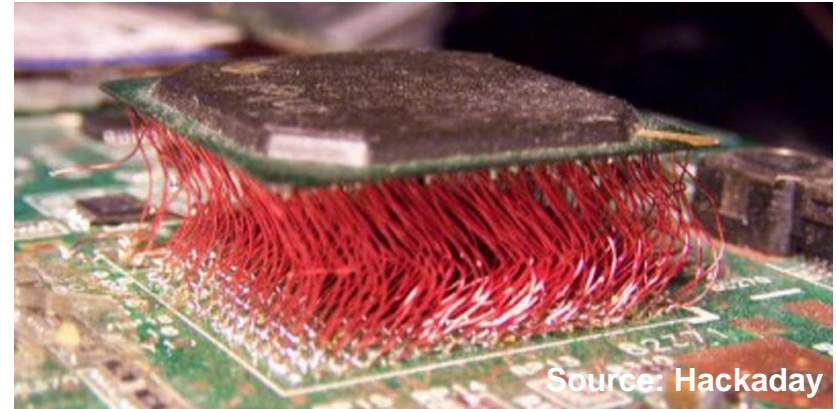
## Data sheet of MicroZed

- **FPGA chip – Zynq™-7000 AP SoC (XC7Z010-CLG400-1)**
  - CPU: Dual **ARM® Cortex™-A9 MPCore™ @ 866 MHz**
  - fast internal static memory 256 kB
  - 4400 slices - *each slice is small configurable logic circuit.*  
*It can create up to 8 flip-flops and 4 logic functions with 6-inputs.*  
*User can freely configure them and mutually interconnect.*
- External dynamic memory – **1 GB DDR3**
- Communication – 10/100/1000 **Ethernet**
- MicroSD card **4 GB**. *In APO board, it contains the loader of Linux system for Ethernet network.*
- **USB Host 2.0 and USB-UART**
- Quad-SPI Flash 128 Mb for power-up initialization.  
*In APO, it is not used.*

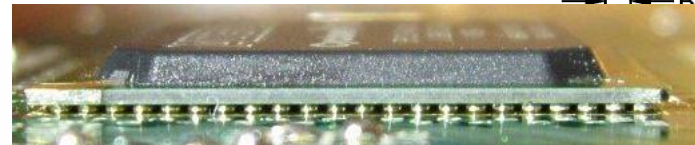
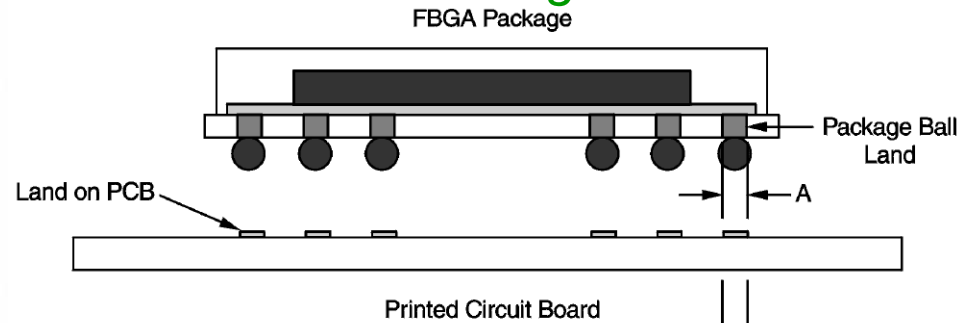
# Zynq™-7000 in FBGA Package

**FBGA** = Fine-Pitch Ball Grid Array

*Clumsy method of FBGA soldering* ☹️



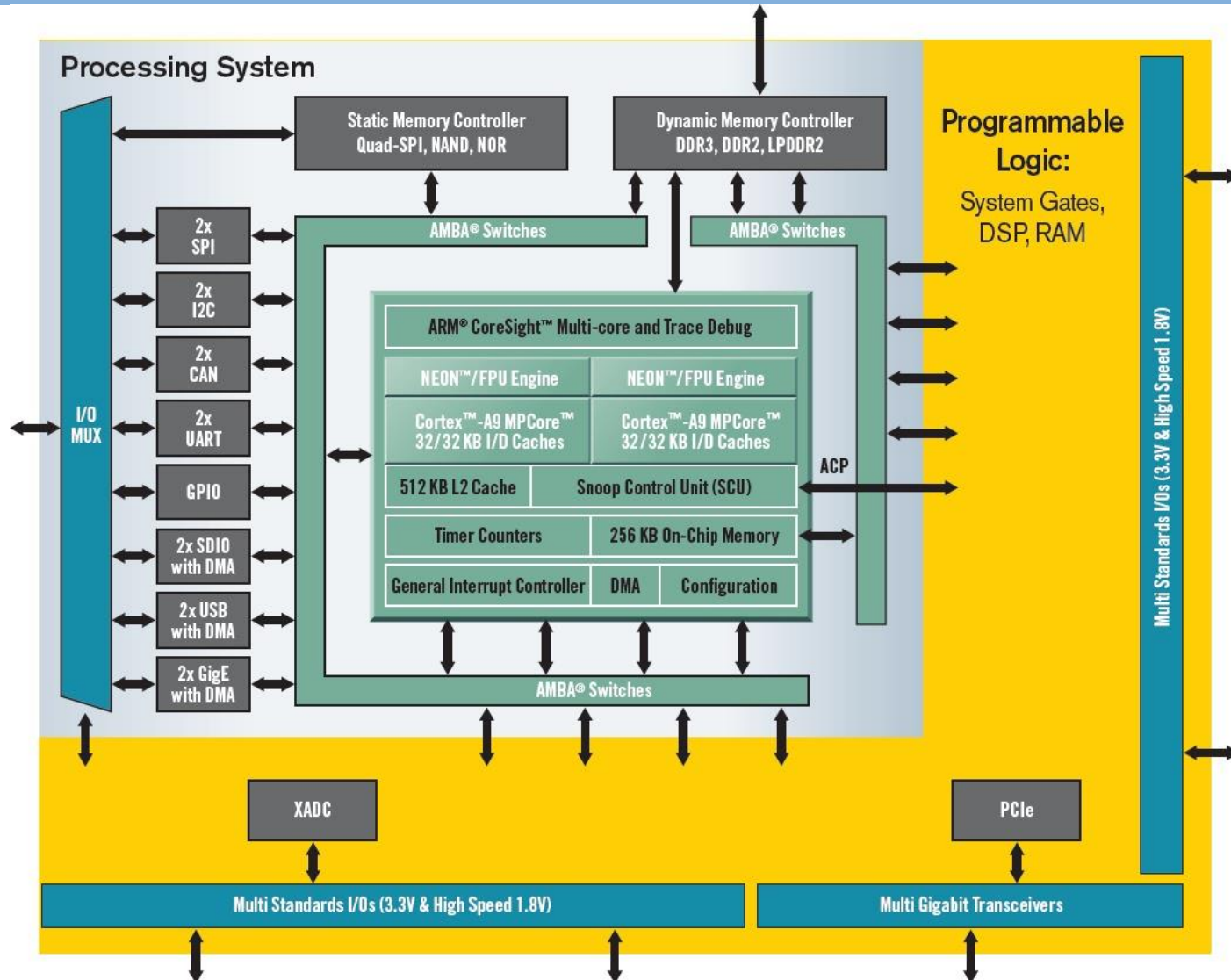
*Intended soldering* 😊



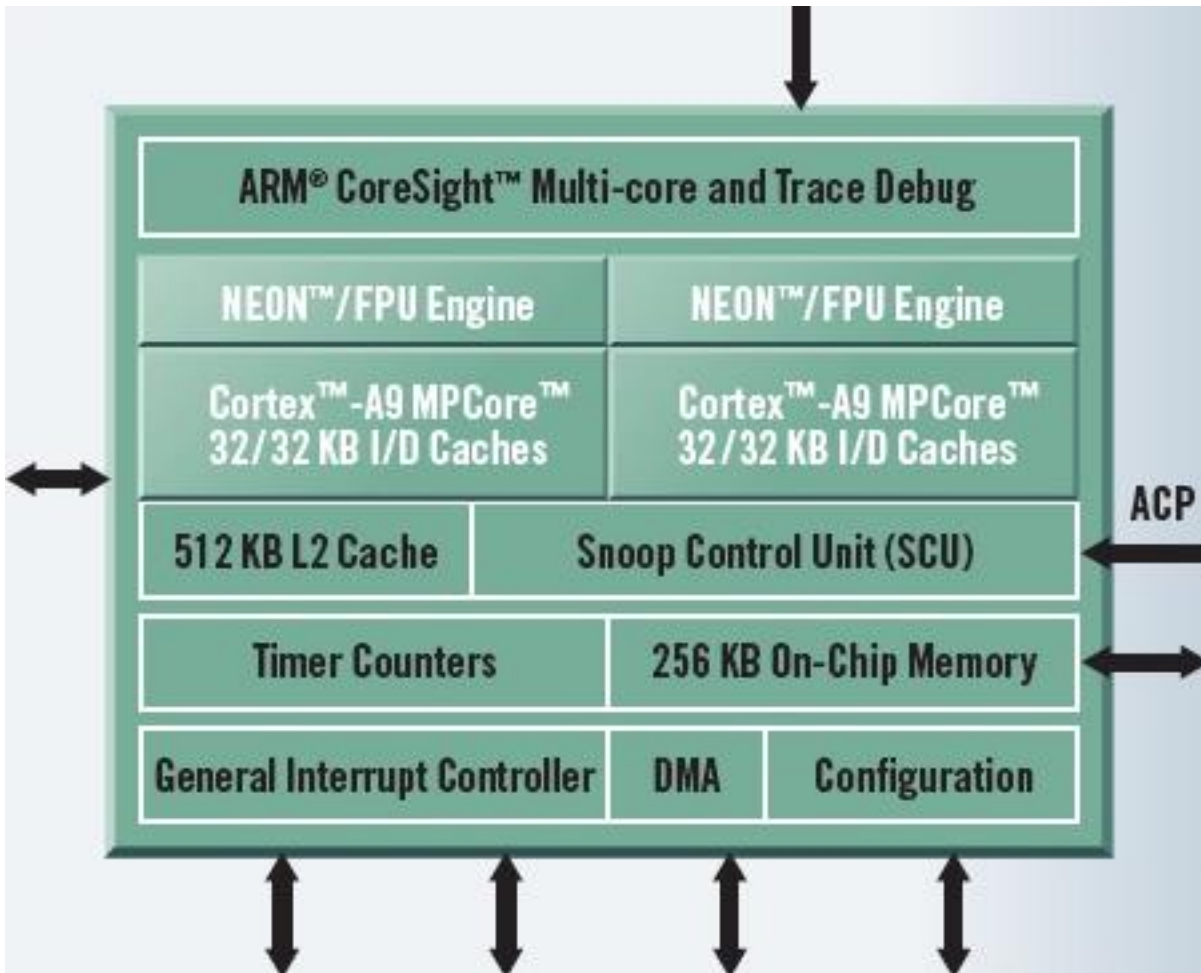
Source: Fairchild Semiconductors



# Inside of Xilinx Zynq™-7000



# Enlarged Zynq Processor Cores



We have already discussed in the lectures:

1. FPU Engine
2. Processor core
3. L1 Instruction/Data caches
4. L2 cache
5. Snoop Control Unit (cache coherency)
6. On-Chip Memory (static RAM)
7. DMA (direct memory access control)

# Where is Cortex-A9 used? Some samples

Apple A5 (iPhone 4S, iPad 2, iPad mini)

[http://en.wikipedia.org/wiki/Iphone\\_4s](http://en.wikipedia.org/wiki/Iphone_4s)



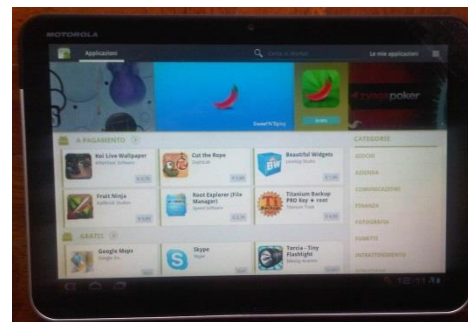
Asus Transformer Pad  
Infinity (TF700T)

[https://en.wikipedia.org/wiki/Asus\\_Transformer\\_Pad\\_Infinity](https://en.wikipedia.org/wiki/Asus_Transformer_Pad_Infinity)



NVIDIA Tegra 2 (Motorola Xoom, Droid X2)

[http://en.wikipedia.org/wiki/Motorola\\_Xoom](http://en.wikipedia.org/wiki/Motorola_Xoom)



Full list see: [https://en.wikipedia.org/wiki/ARM\\_Cortex-A9#Implementations](https://en.wikipedia.org/wiki/ARM_Cortex-A9#Implementations)

# CortexA9 Microarchitecture

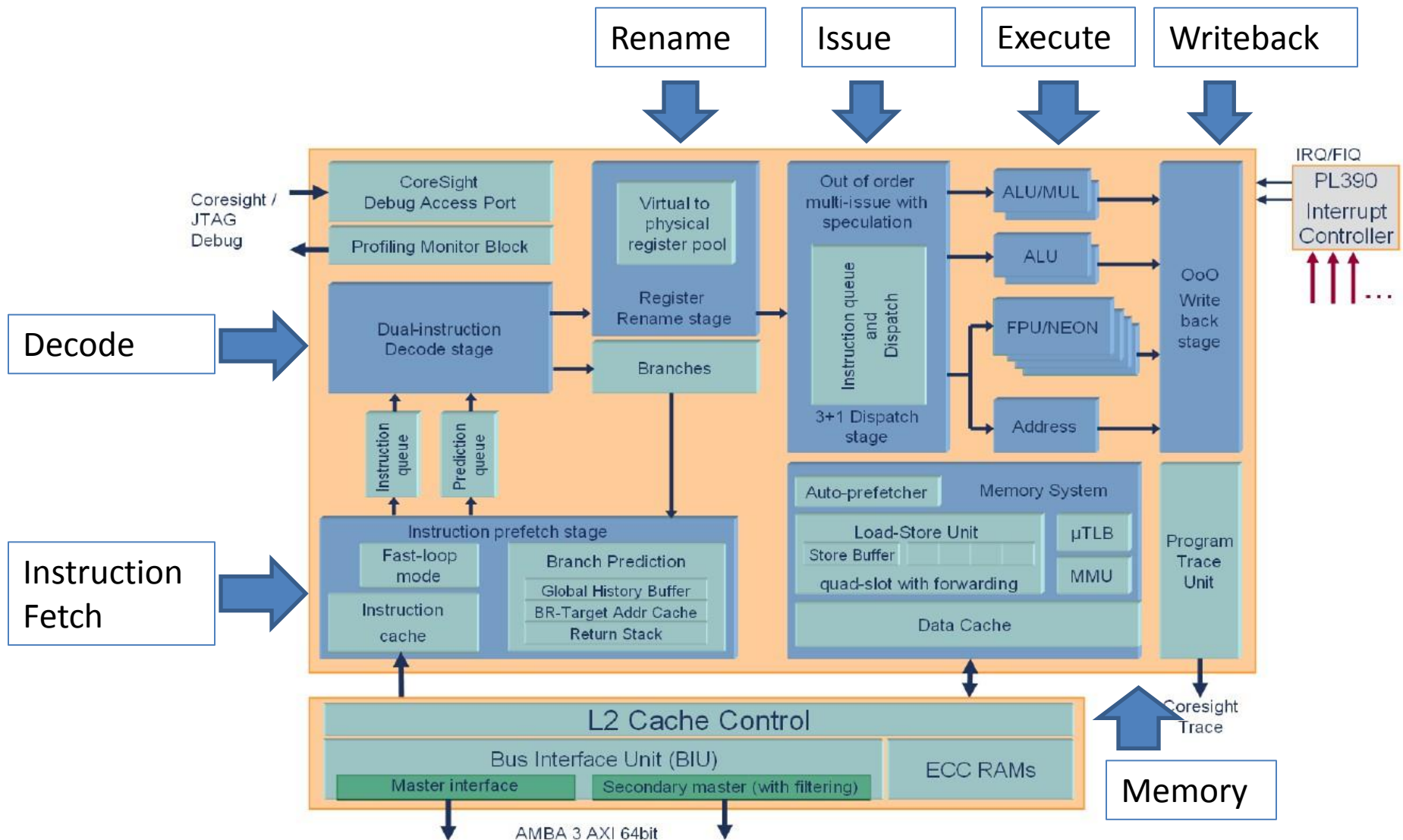


Fig. 1 Cortex-A9 microarchitecture structure and the single core interfaces.

# Our Cortex A9 MP Core properties

- **32 bit RISC Little Endian**, 16 registers integer
- 2.5 DMIPS/MHz
  - -> 866 MHz \* 2.5 DMIPS/MHz = **2165 DMIPS**
- *Note: DMIPS is the result of Dhrystone synthetic computing benchmark intended to represent integer programming.*
- Most Integer Instructions finish within 1 cycle, integer multiply needs 4 ~ 5 cycles.
- Float point instruction last on ALU from 4 cycles addition, subtraction (FADD, FSUB), 5 cycles multiply FMUL, 15 cycles divide FDIV (3times longer than multiply!), 17 cycle square root FSQRT.
- Branch prediction
  - 4 K entries table of 2 bit predictors.
- **Virtual memory with 2 level paging tables**

# L1 and L2 Caches

**2 separate L1 caches**, for I-cache instructions and D-cache for data.

Both L1 have properties:

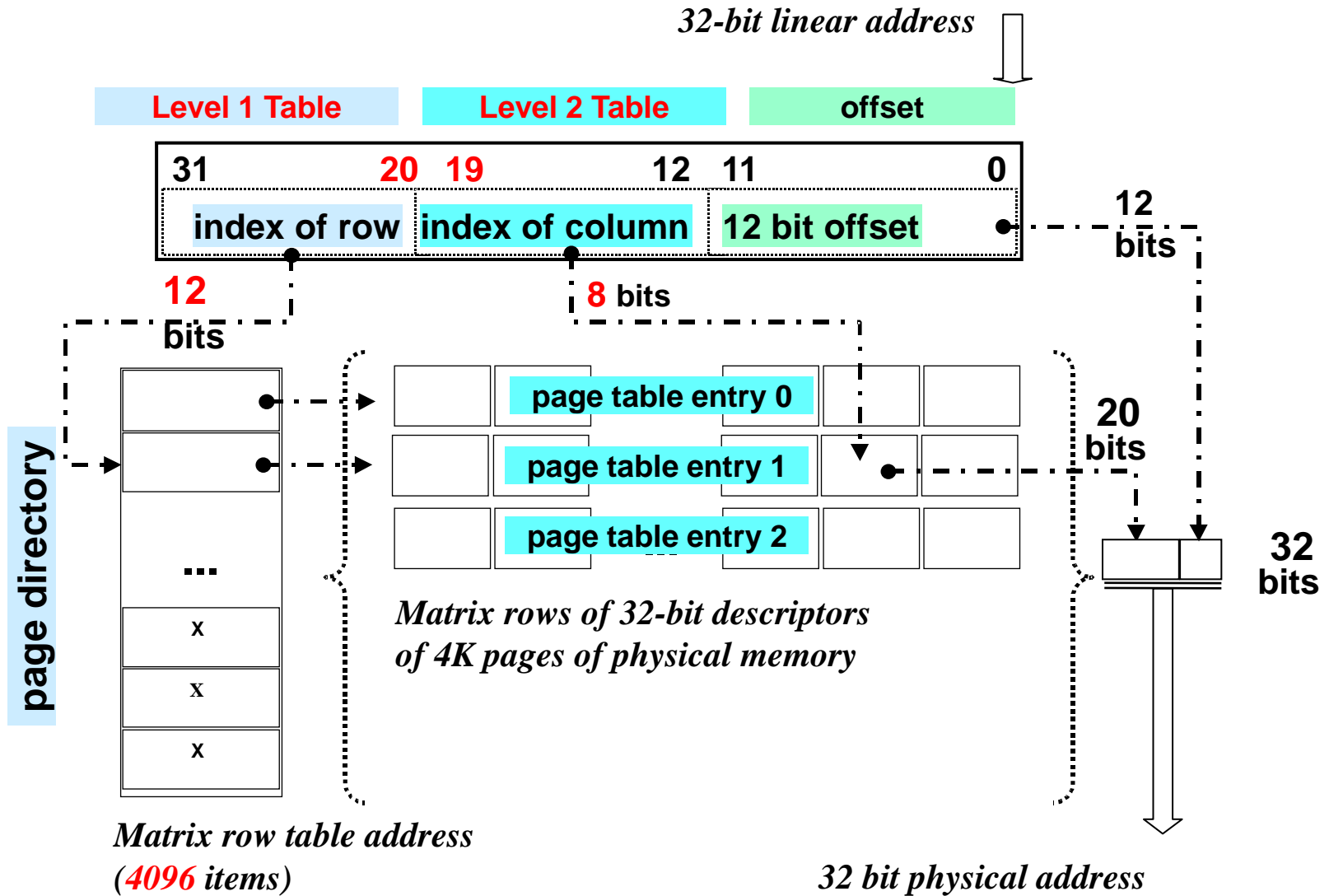
- **32 kB size**,
- 4-way set associative,
- 32 byte block length,
- replacement policy is pseudo-random or pseudo round-robin.
- **D-Cache** only supports write-back/write-allocate policy.

**L2 cache** is shared by dual Cortex-A9 cores. Its properties:

- **512 KB size**,
- 8-way set-associative,
- 32 byte block (line) length,
- replacement policy is pseudo-random,
- supports Write-back,  
and Write-through with Read allocate, Write allocate.



# Cortex A9

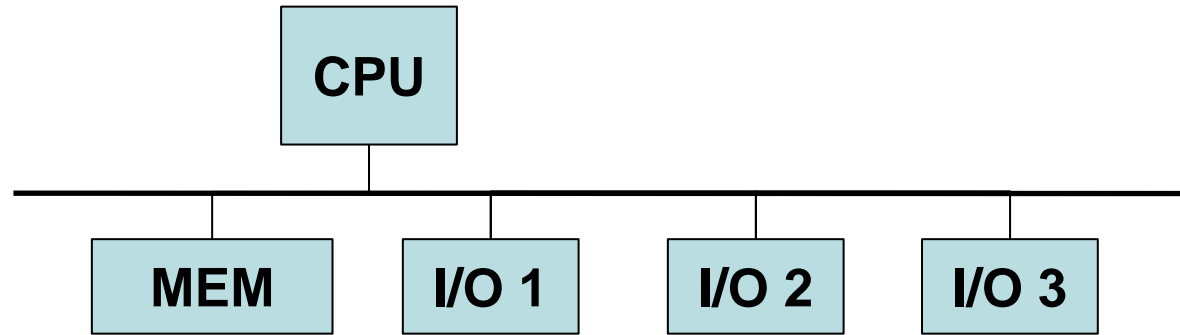




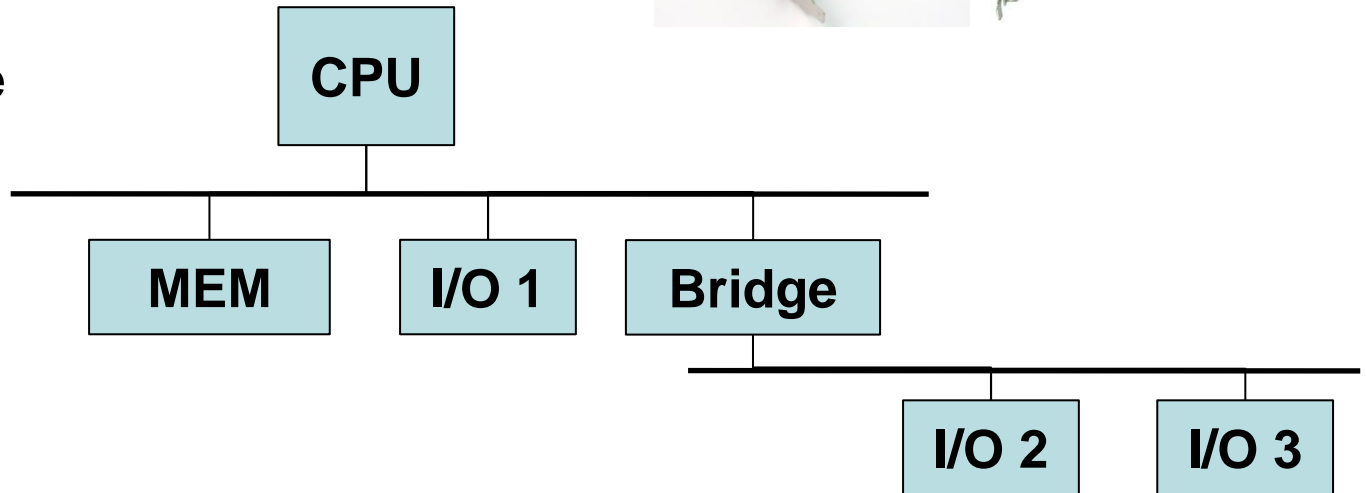
# \* I/O Pheripherals

# Dekodér adres - idea

- Logická struktura: (iluze)

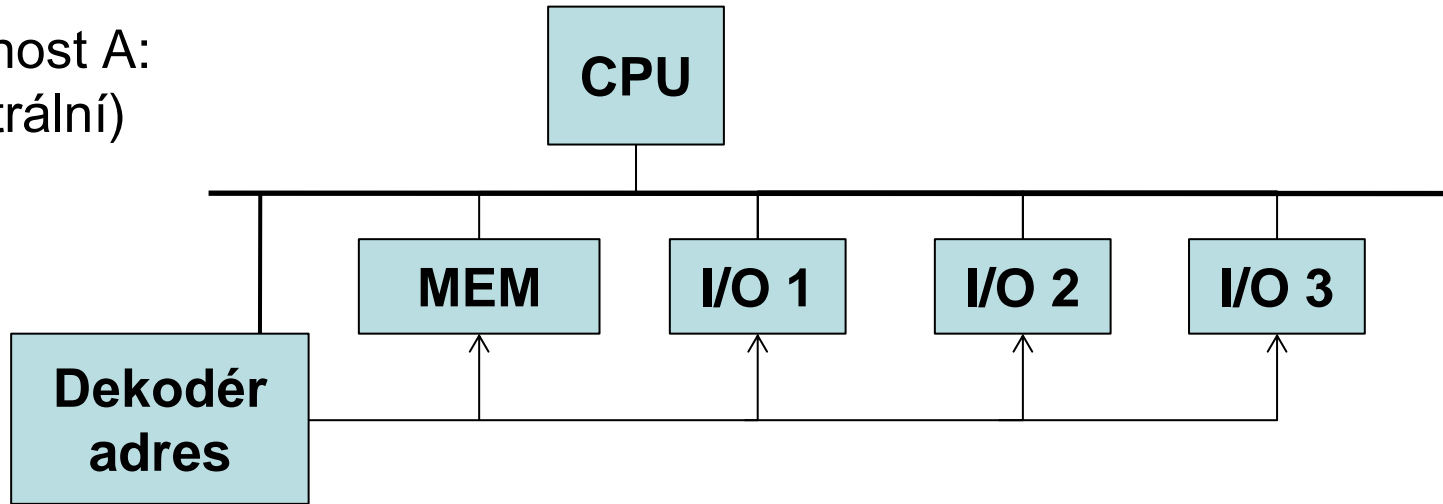


- Možné fyzické uspořádání:

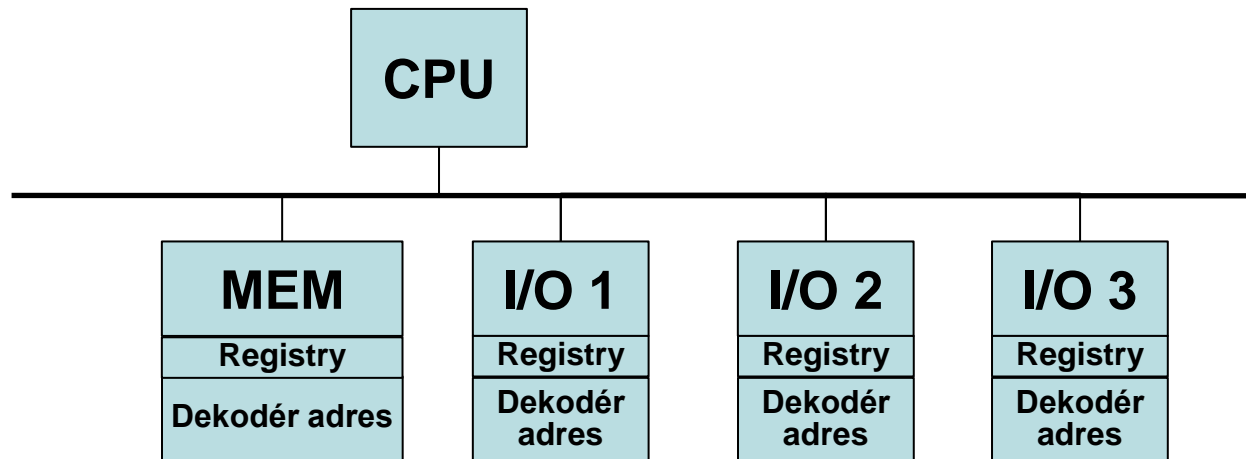


# Dekodér adres - idea

- Možnost A:  
(centrální)



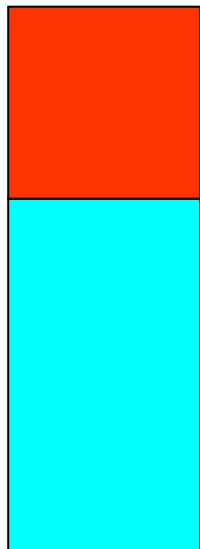
- Možnost B:  
(autonomní)



# Paměťově mapované I/O

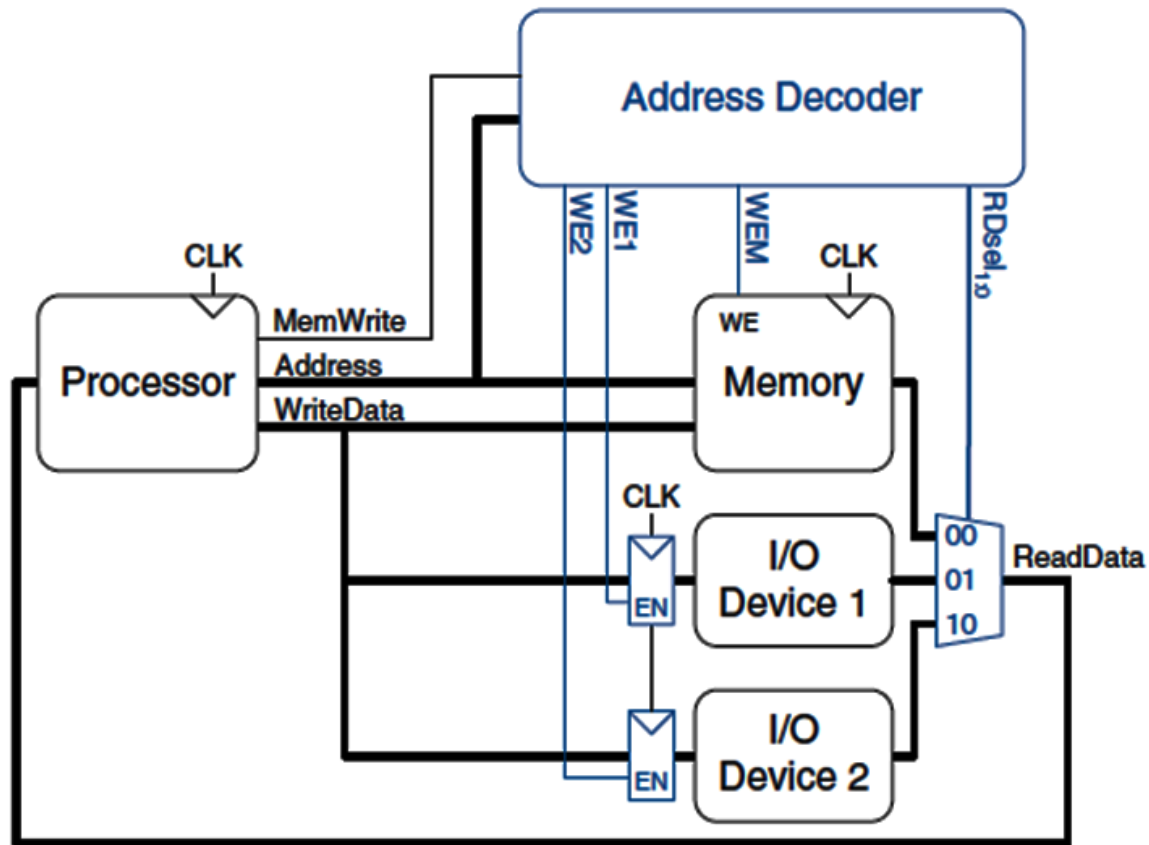
- Idea: K tomu abychom komunikovali s vstupně/výstupními periferiemi (klávesnice, monitor, tiskárna) můžeme použít stejné rozhraní jako pro komunikaci s pamětí (MIPS: instrukce lw, sw).

Společný adresní prostor pro I/O a paměť

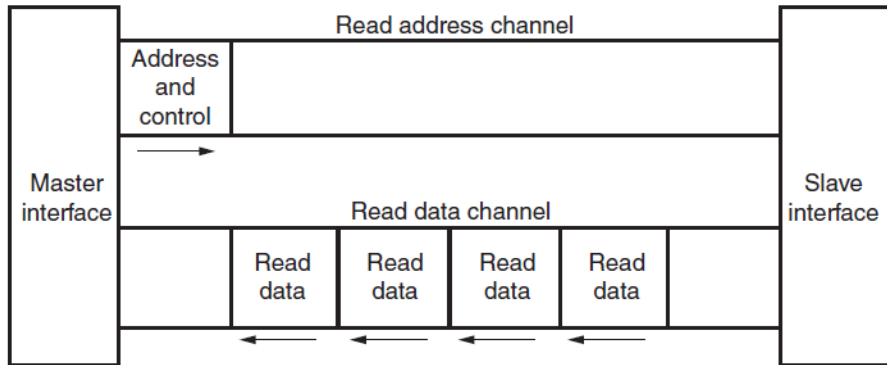


V/V brány jsou mapované do paměti

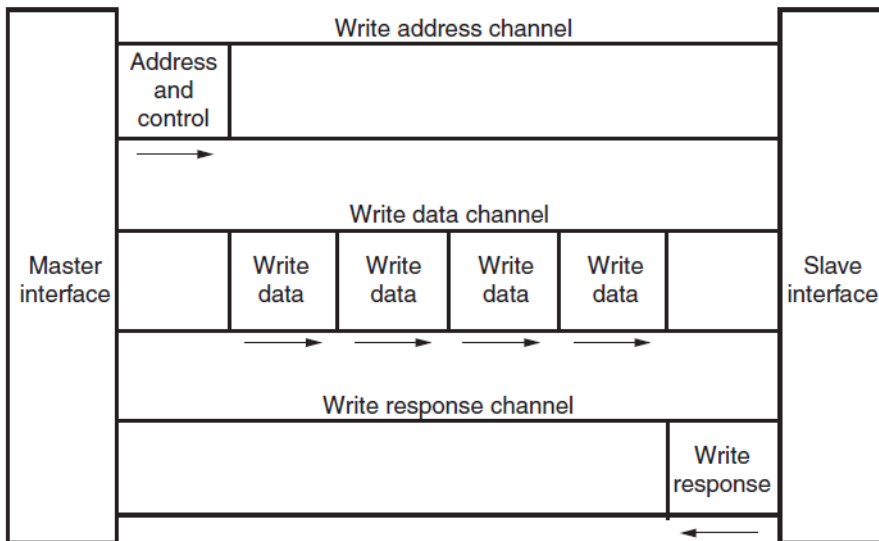
paměť



# MicroZed uses on-chip bus AXI !



X12076



**Advanced eXtensible Interface (AXI)** consists of five different channels:

- Read Address Channel
- Read Data Channel
- Write Address Channel
- Write Data Channel
- Write Response Channel

*On-chip buses are used only inside integrated circuits and utilize switching multiplexors that allow simultaneous reading and writing operations.*

*They will be described by LSP course (the next semester).*

**External PC buses (ISA, PCI, SATA, PCIe) have different operation! We will deal with them in a future lecture.**

# Design of Peripherals in Xilinx Vivado

The screenshot displays the Xilinx Vivado IDE interface for a Block Design project. The main window shows a diagram of a ZYNQ Processing System (processing\_system7\_0) connected to several peripheral blocks via an AXI Interconnect. The peripherals include:

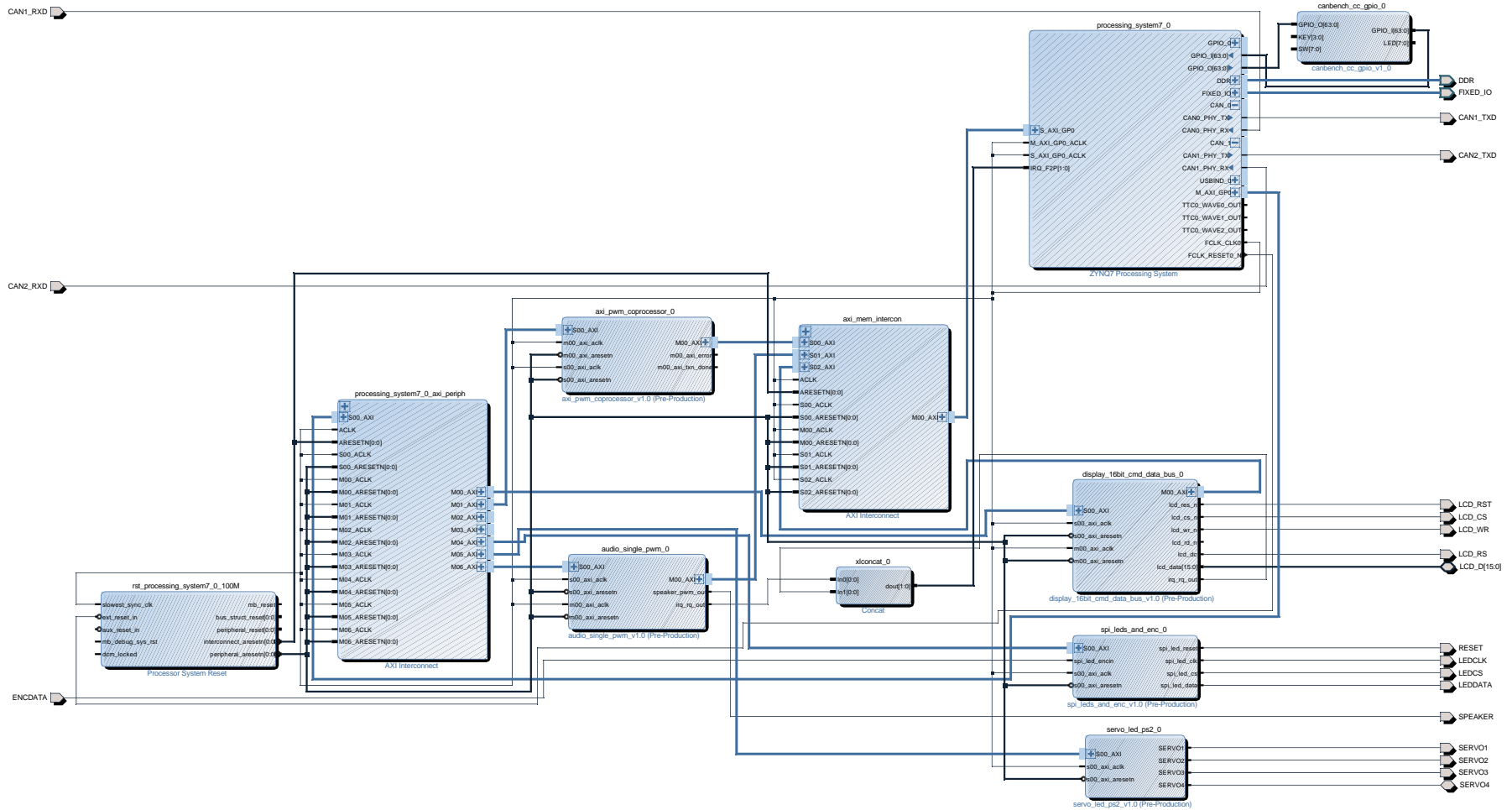
- axi\_mem\_intercon**: AXI Interconnect block.
- display\_16bit\_cmd\_data\_bus\_0**: Display controller block.
- canbench\_cc\_gpio\_0**: GPIO controller block.
- canbench\_cc\_gpio\_v1\_0**: GPIO controller block.
- lcd**: LCD controller block.

The diagram shows the ZYNQ Processing System with various pins connected to these peripherals. The AXI Interconnect is connected to the processing system and the display controller. The GPIO controller blocks are connected to the processing system and the display controller. The LCD controller is connected to the processing system and the display controller.

The left sidebar shows the Project Manager and IP Integrator sections. The Project Manager shows the project settings, and the IP Integrator shows the list of IP blocks used in the design. The bottom panel shows the Tcl Console with the following output:

```
Adding cell -- xilinx.com:ip:axi_protocol_converter:2.1 - auto_pc
Adding cell -- xilinx.com:ip:axi_protocol_converter:2.1 - auto_pc
Adding cell -- xilinx.com:ip:axi_protocol_converter:2.1 - auto_pc
Adding cell -- xilinx.com:ip:axi_protocol_converter:2.1 - auto_pc
Successfully read diagram <top> from BD file </home/pi/fpga/zyng/canbech-sw/system/src/top/top.bd>
open_bd_design: Time (s): cpu = 00:00:24 ; elapsed = 00:00:19 . Memory (MB): peak = 6008.051 ; gain = 153.621 ; free physical = 80 ; free virtual = 7868
set_property location {-22 483} [get_bd_ports CAN2_RXD]
set_property location {-26 1138} [get_bd_ports ENCDATA]
write_bd_layout -format pdf -orientation portrait /home/pi/mz_apo-v10-top.pdf
/home/pi/mz_apo-v10-top.pdf
```

# Vivado Design of Peripherals for APO



Complete design sources: [https://cw.fel.cvut.cz/b182/courses/b35apo/documentation/mz\\_apo/start](https://cw.fel.cvut.cz/b182/courses/b35apo/documentation/mz_apo/start)

# MicroZed Physical Memory

Address start	Length	
0x0000 0000	1 GB	DRAM
0x4000 0000	1 GB	AXI bus port 0 to FPGA
0x43c00000	16 bytes	APOZed - LCD display
0x43c40000	48 bytes	APOZed - Peripherals
0x8000 0000	1 GB	AXI bus port 1 to FPGA
0xE000 0000		Reserved for system
0xFFFC 0000	256 kB	On chip static memory

But Cortex A9 runs with GNU/Linux OS that is configured for paging, thus, we **cannot** use directly physical addresses!



# Mapping Hardware in Linux

*It is simplified part of the code that you use in your semester project*

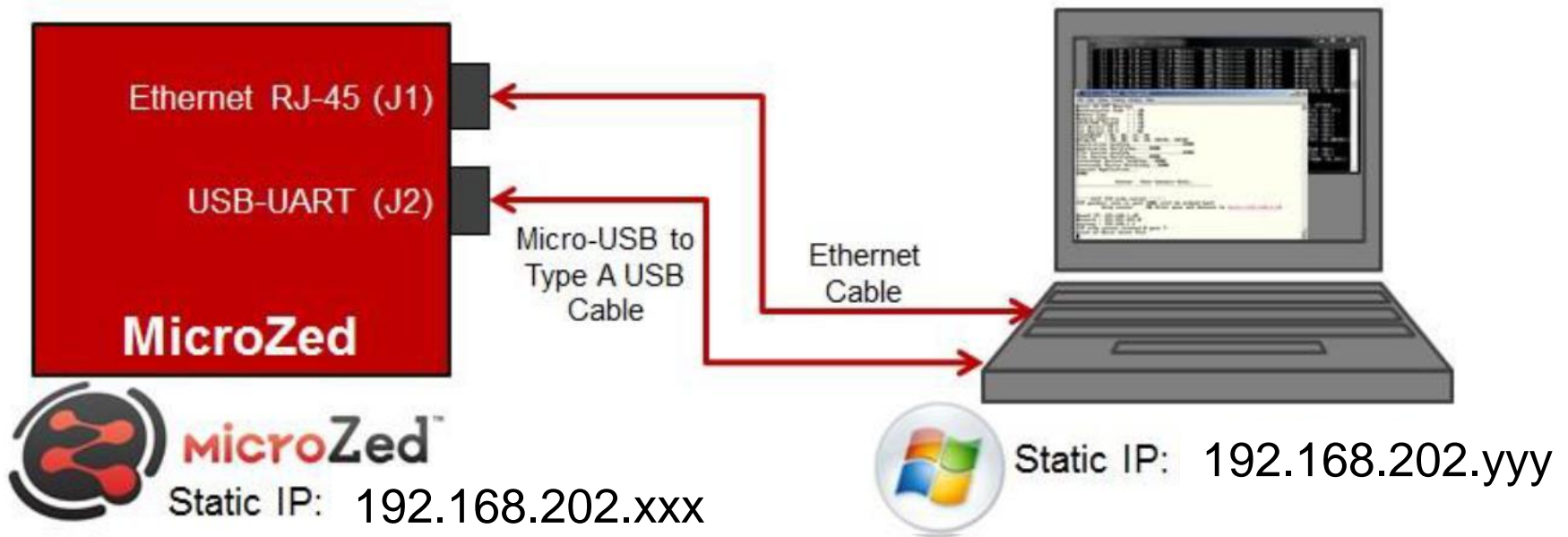
```
int fd = open("/dev/mem", /* we ask for physical memory addresses */
             O_RDWR /* with read and write access */
             | O_SYNC /* and non-cached for /dev/mem */
             );
unsigned char *mem = (unsigned char *) mmap(
    NULL, /* kernel selects virtual address */
    0x4000 /* our required size = MicroZed physical mem view */,
    PROT_READ | PROT_WRITE, /* allow read and write*/
    MAP_SHARED, /* visible to other processes*/
    fd, /* handle of an already opened file */
    0x43c40000 /* offset in file, here I/O physical base address*/ );
```

*Note: For simplification, we have supposed that the size and offset are already align to page size.*

*Full template: [https://gitlab.fel.cvut.cz/b35apo/mzapo\\_template](https://gitlab.fel.cvut.cz/b35apo/mzapo_template)*

# \*Connecting to the board

# Connection to Board

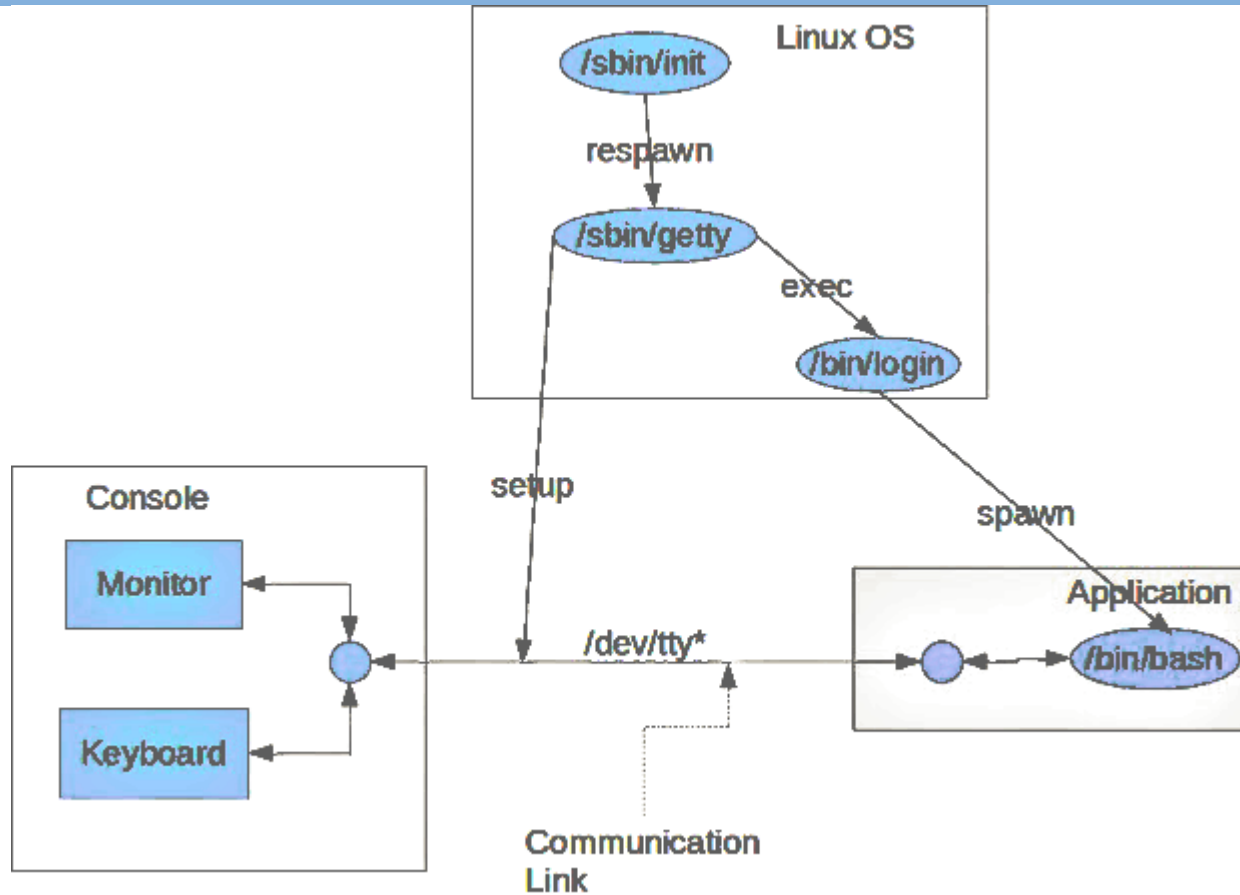


## Notes:

1. *Micro USB is replaced by more robust USB type B on our carry board.*
2. *In Linux,*
  - *GtkTerm allows USB connection*
  - *SSH utilizes Ethernet*



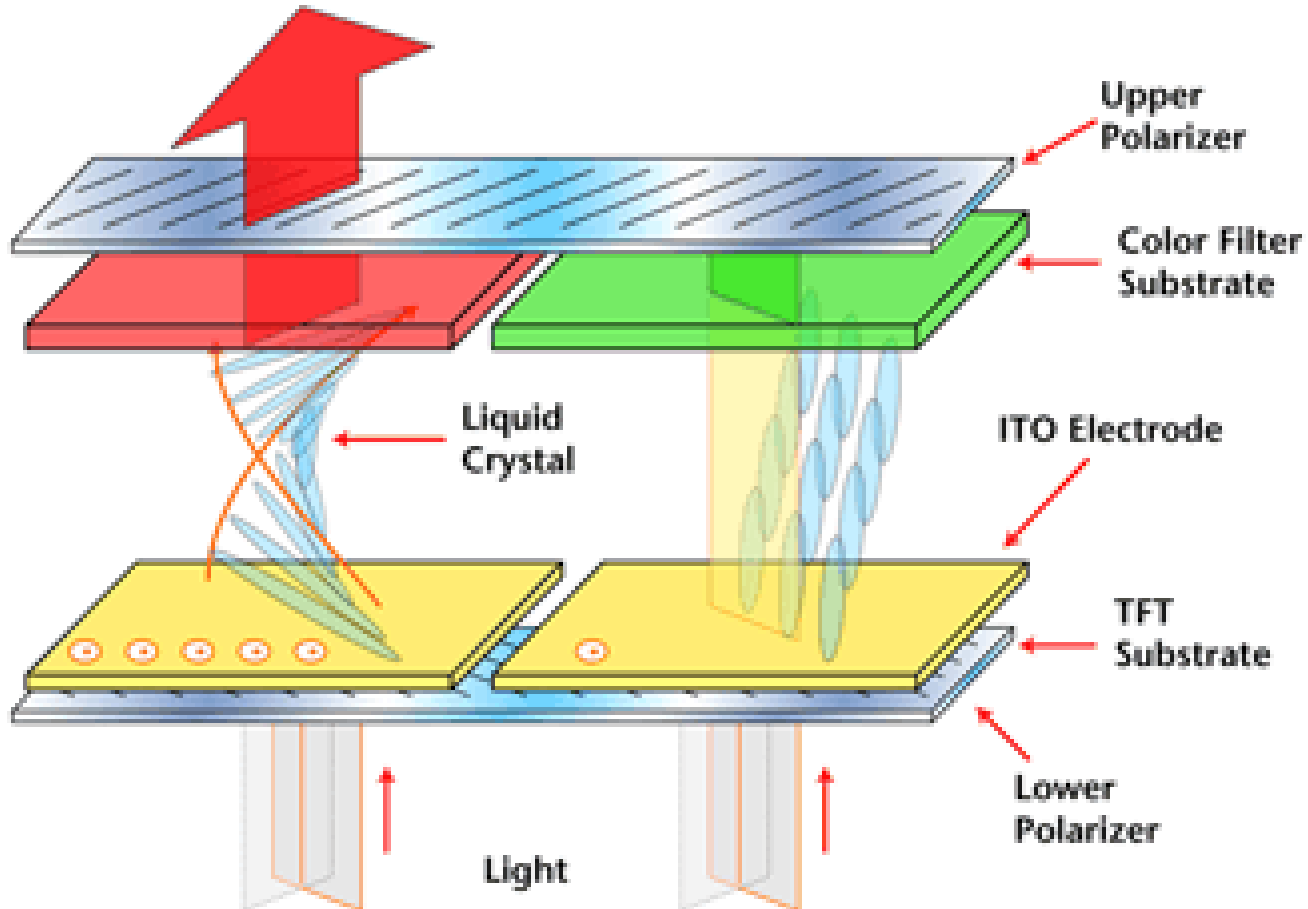
# Linux Console Concept



- GtkTerm uses `/dev/ttyUSB0`
- SSH connect through Ethernet and uses `/dev/tty*`

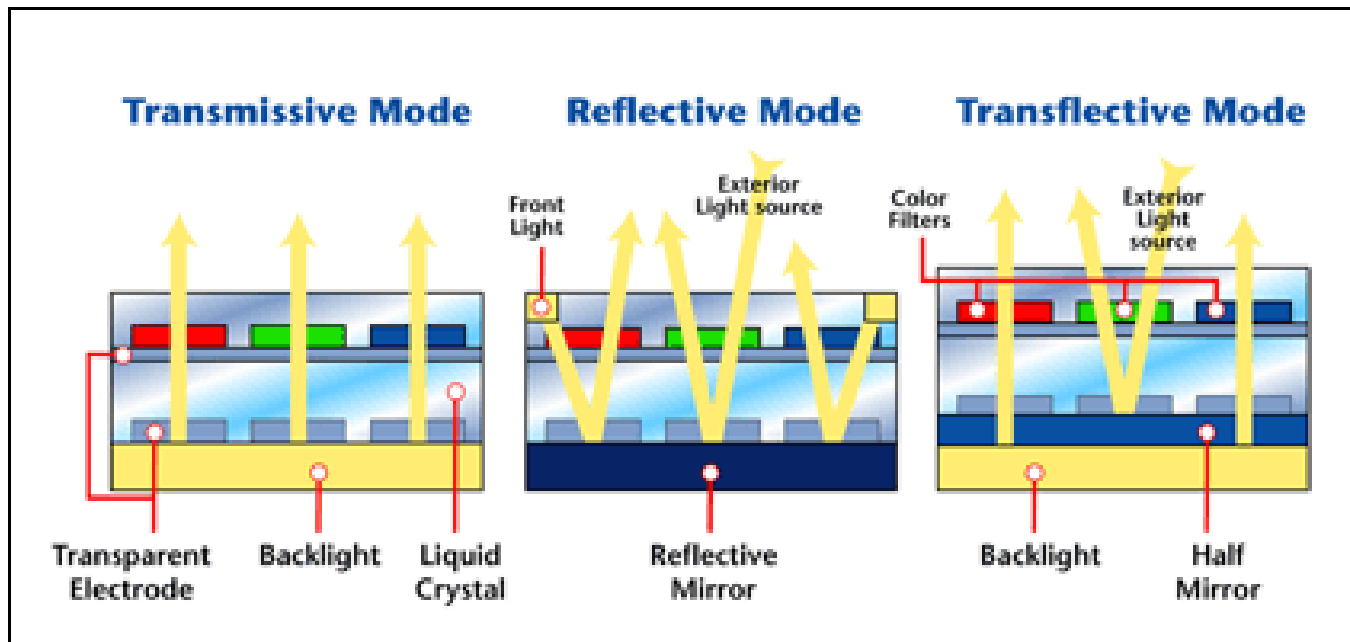
# \*LCD display

# LCD Lighting Theory



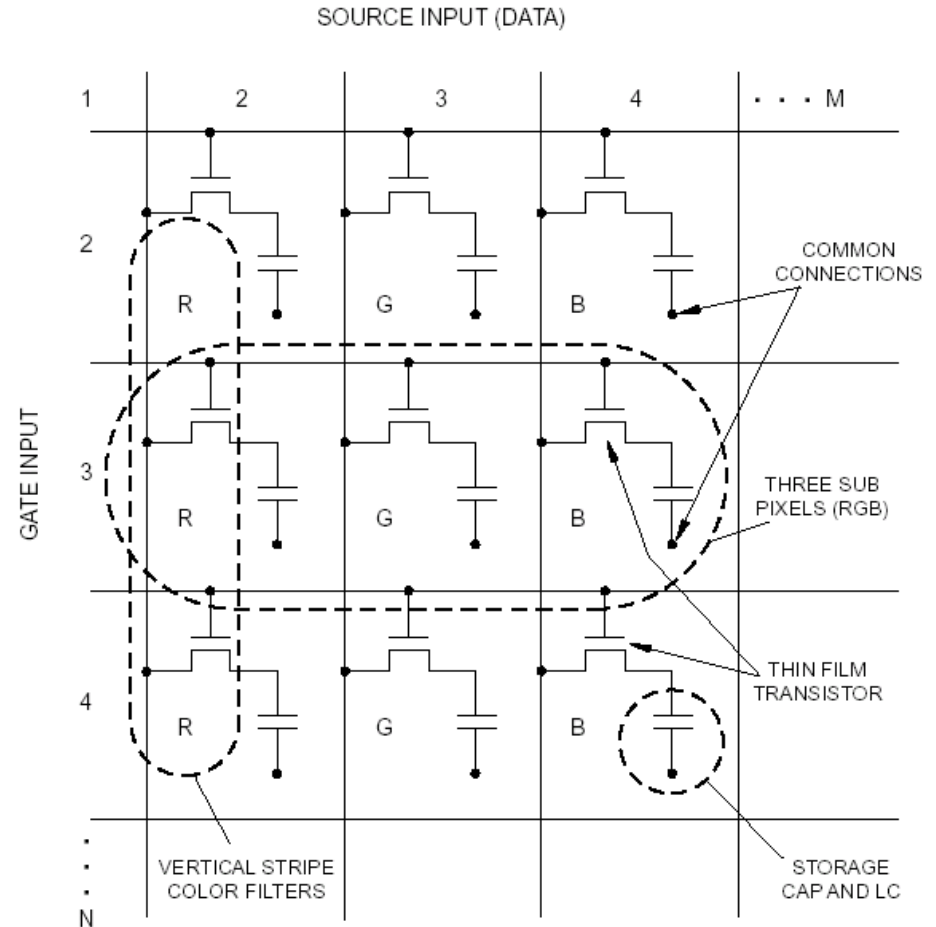
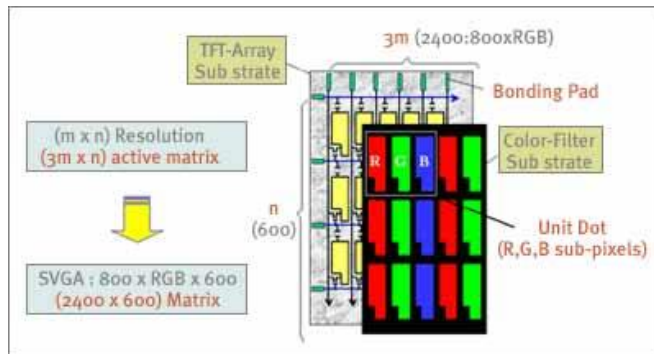
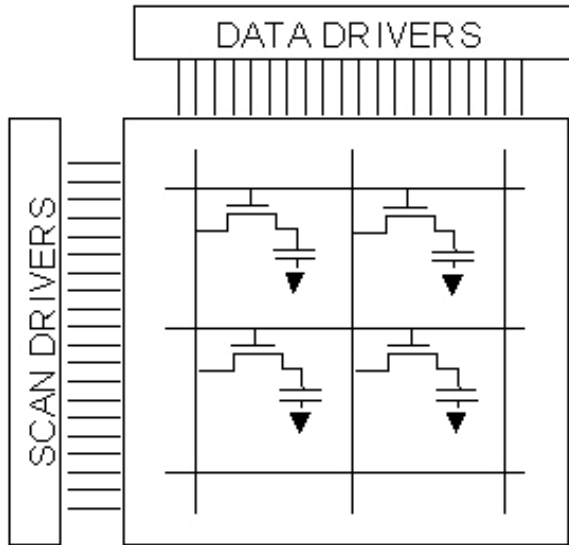
Source: 

# LCD Lighting Theory



Source: 

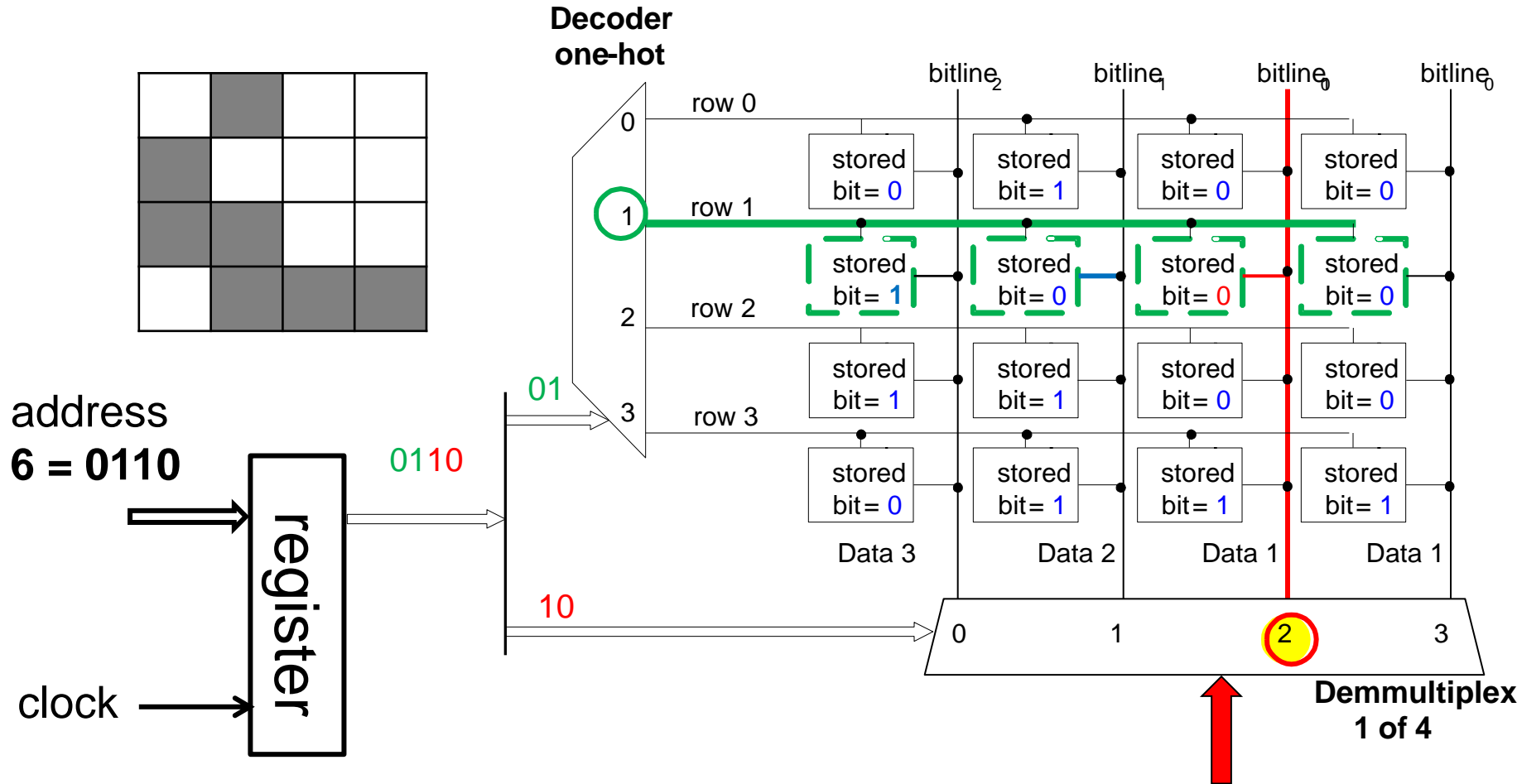
# TFT with Active Matrix



Source: 



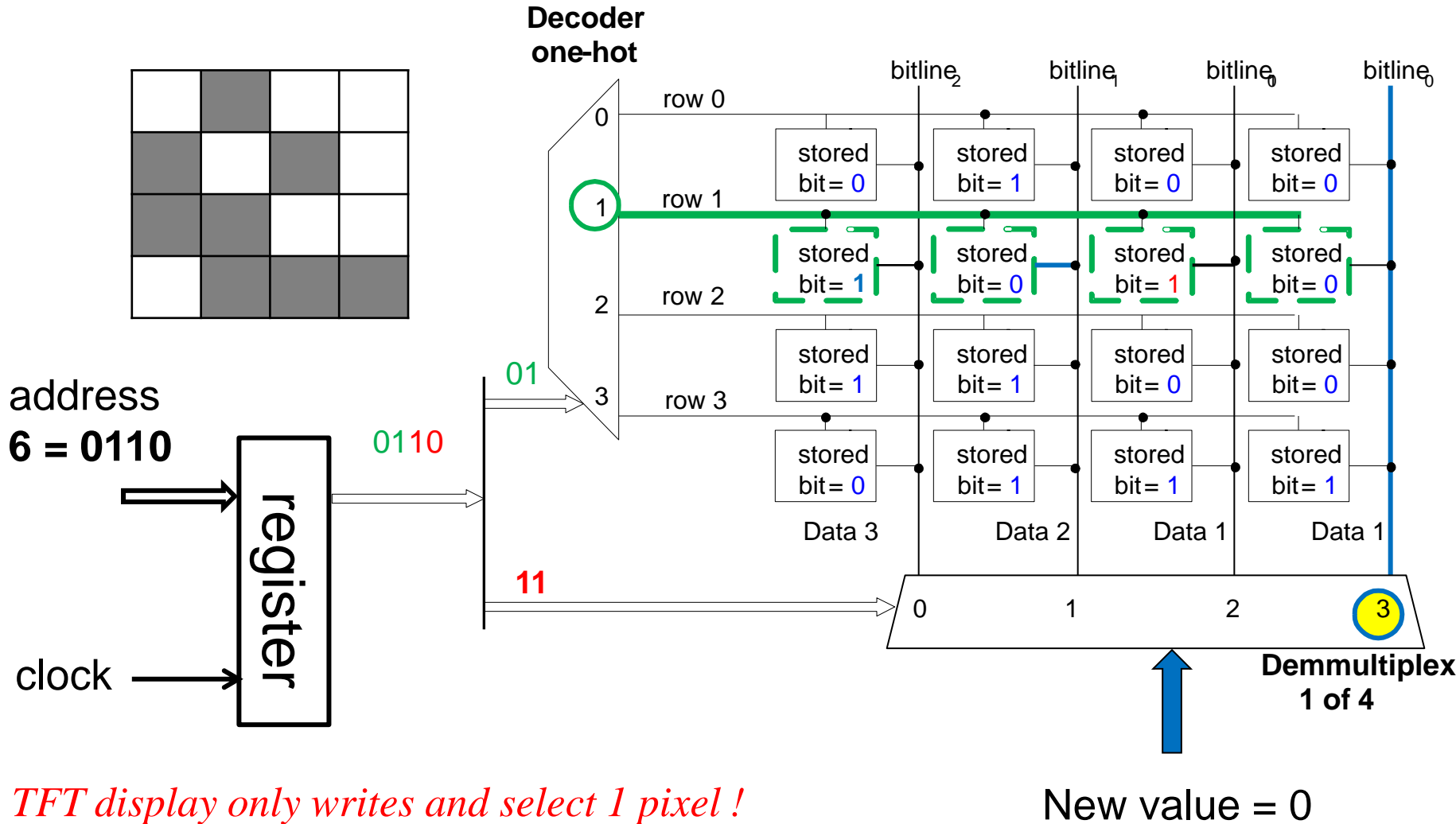
# Compare with Memory Matrix from 4th lecture



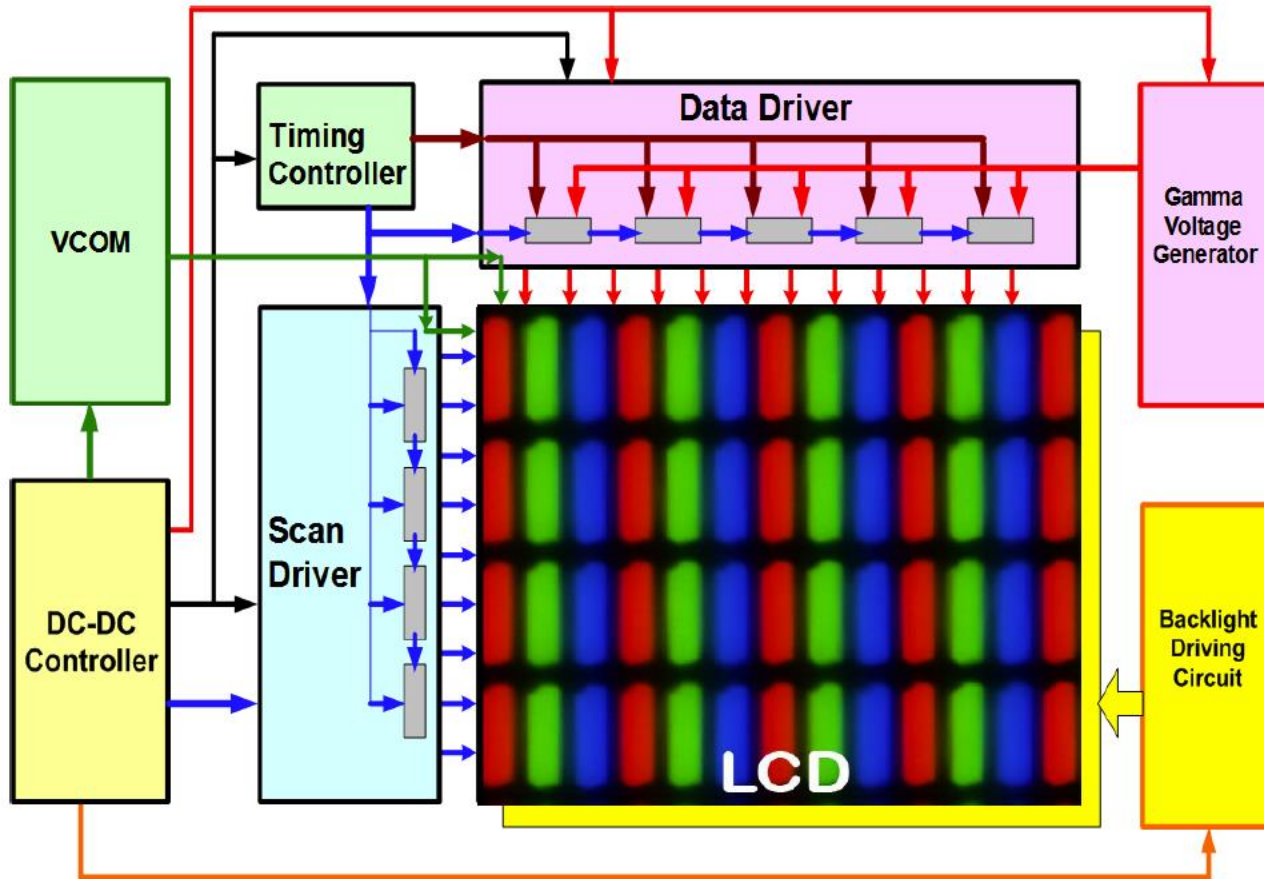
*TFT display only writes and usually selects only 1 pixel !*

New value = 1

# Compare with Memory matrix 4th lecture



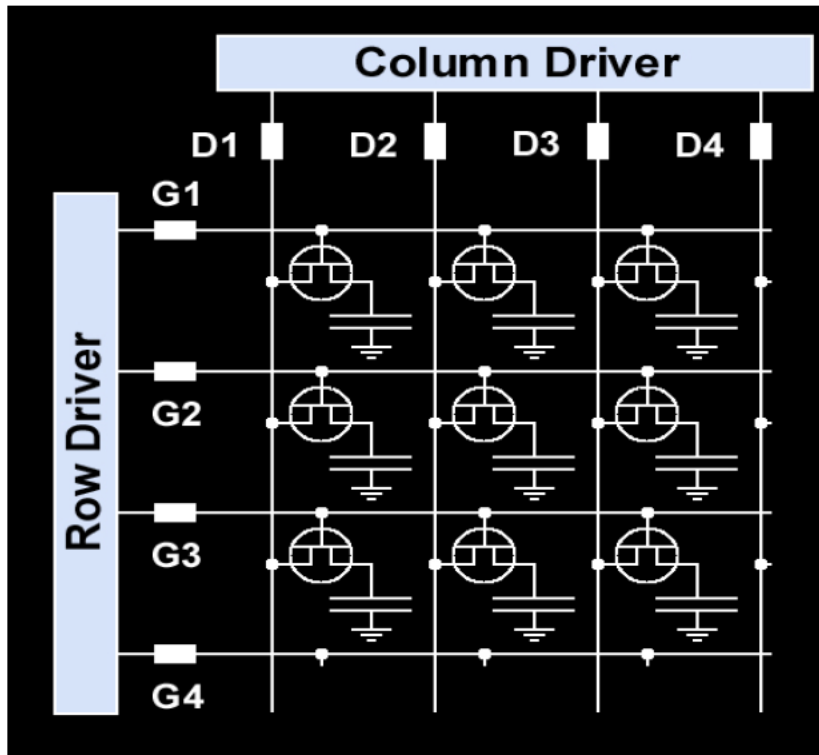
# LCD Control



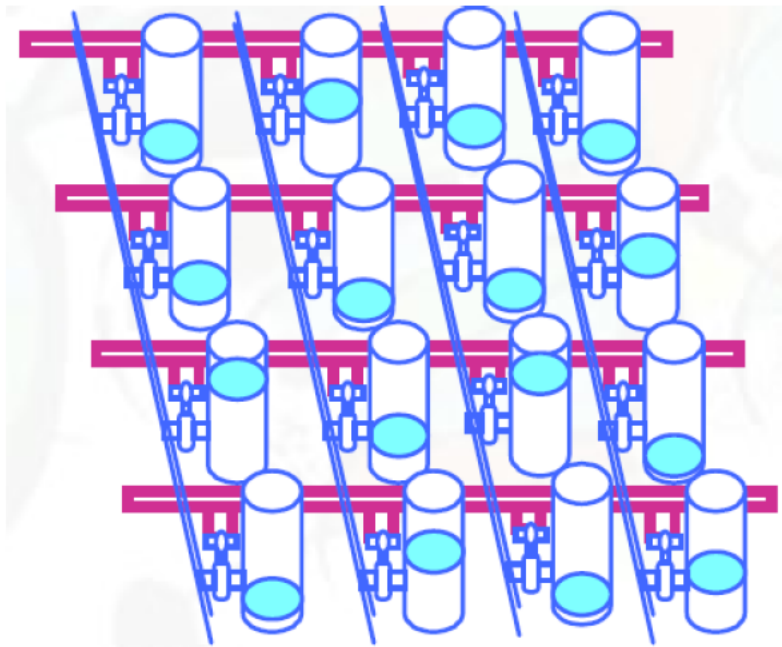
Source: Dr. Zhibing Ge, College of Optics and Photonics

# LCD Pixel has More Levels !

TFT (switch) + LC cell (capacity)

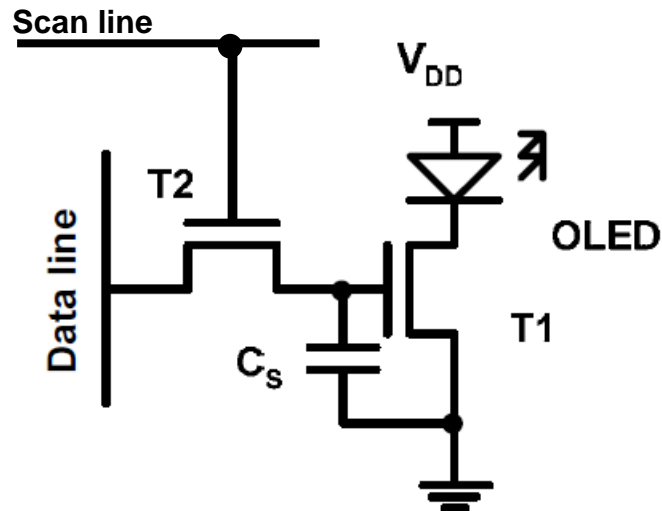
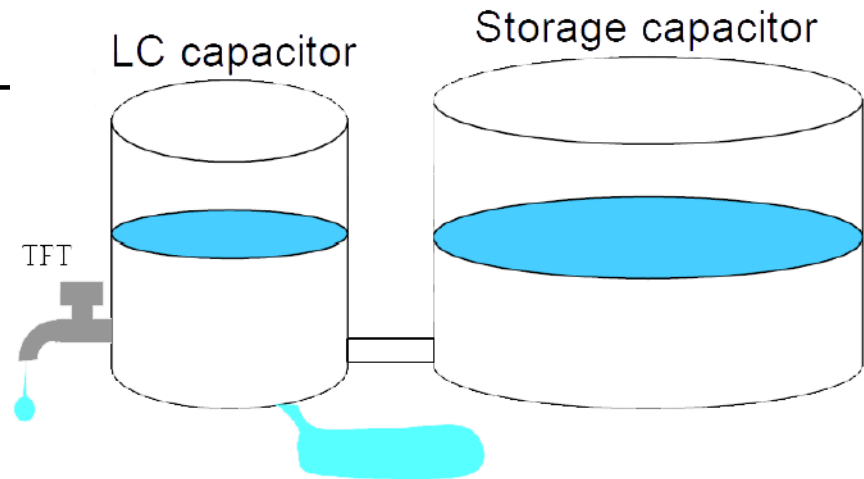
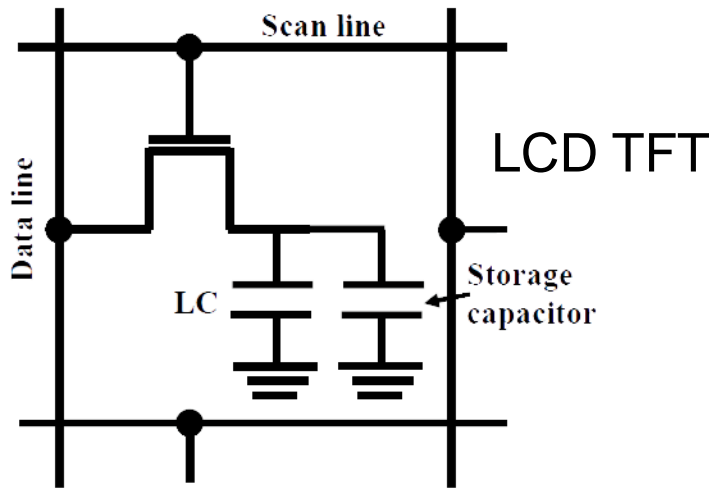


Hydrant (switch)+ Bucket (capacity)



Source: Dr. Zhibing Ge, College of Optics and Photonics

# LCD Refreshing



LCD display needs periodic refresh as DRAM, but in slower rate. Typical values of  $C_s$  are from 100 fF (=0.1pF) to 2000 fF (=2pF), in DRAM from 10 to 50 fF.

## LCD read/write

Our program contains assembler instruction of compiled C code

```
register1 = * address;
```

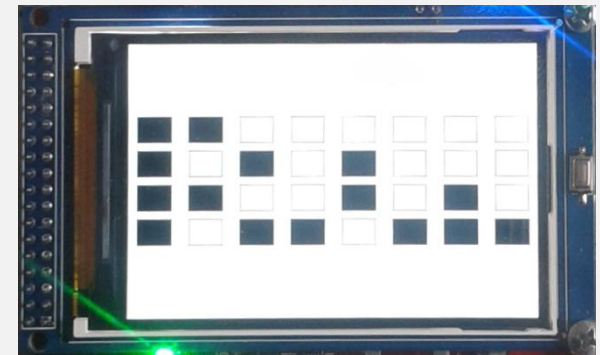
or

```
* address = register2;
```

Program in DDR3  
rd/wr virtual address

APO MicroZed

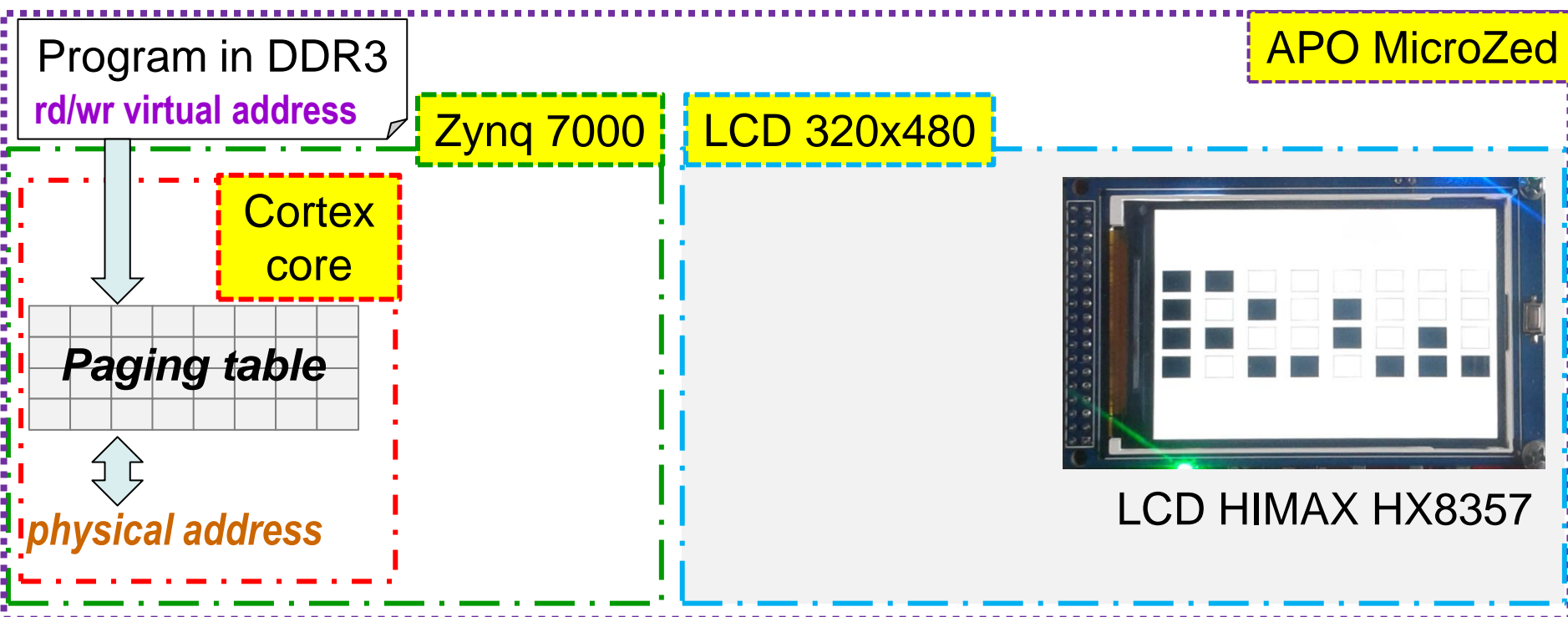
LCD 320x480



LCD HIMAX HX8357

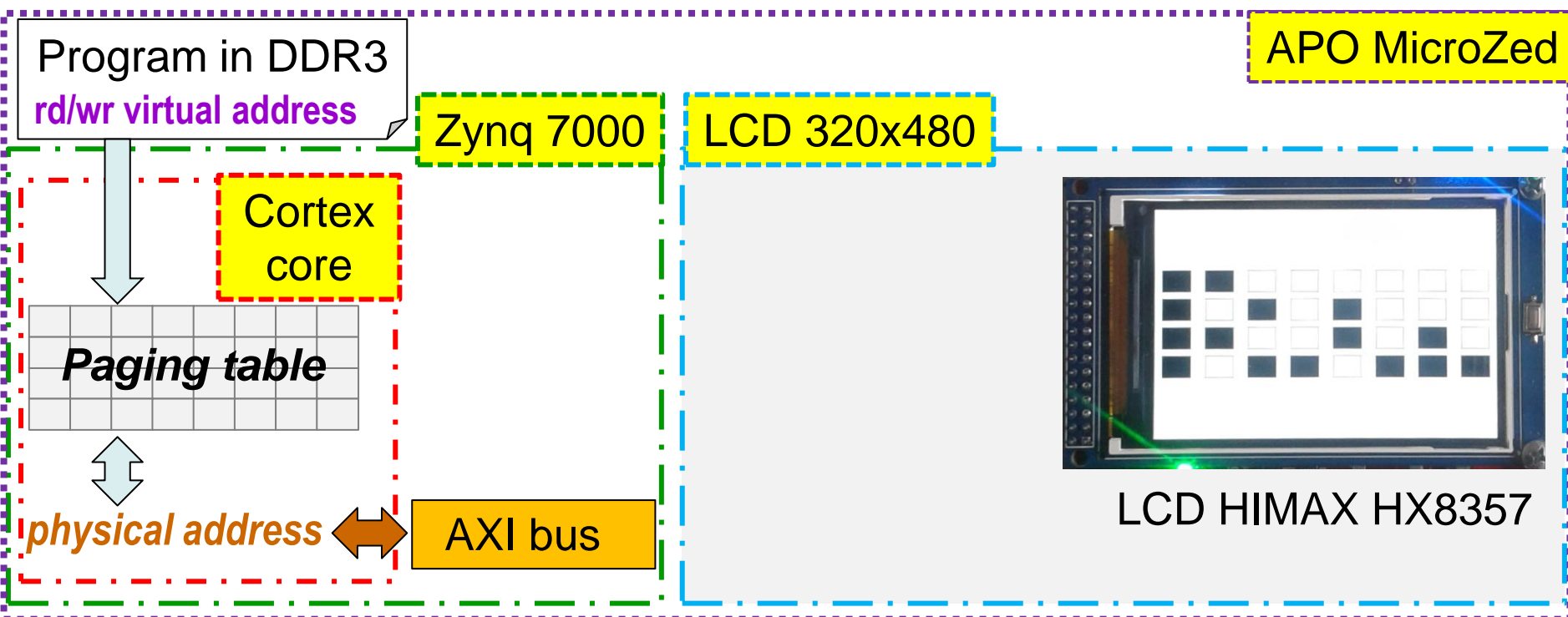
# LCD read/write

Virtual address is transformed to physical address during FETCH phase of pipeline



# LCD read/write

Physical address and data are send to AXI bus

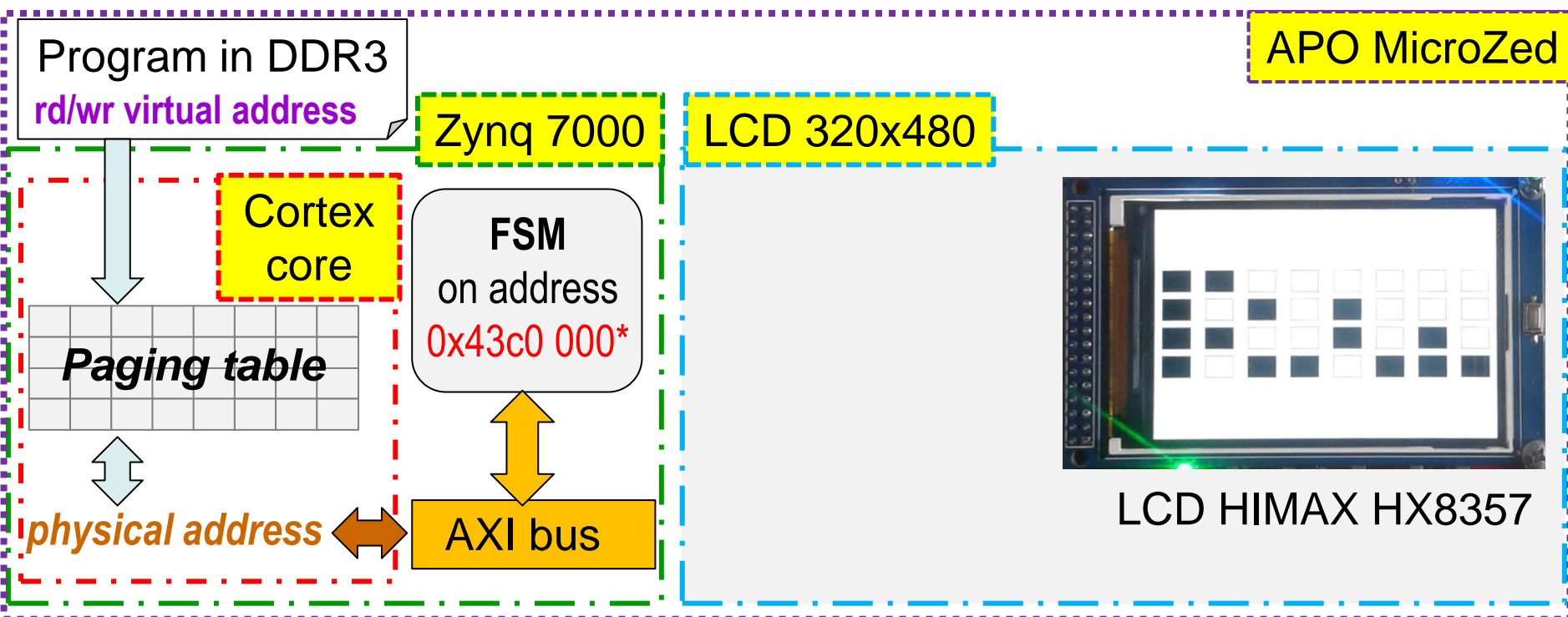




# LCD read/write

**FSM** (Finite State Machine, cz: konečný automat) compares addresses on AXI bus.

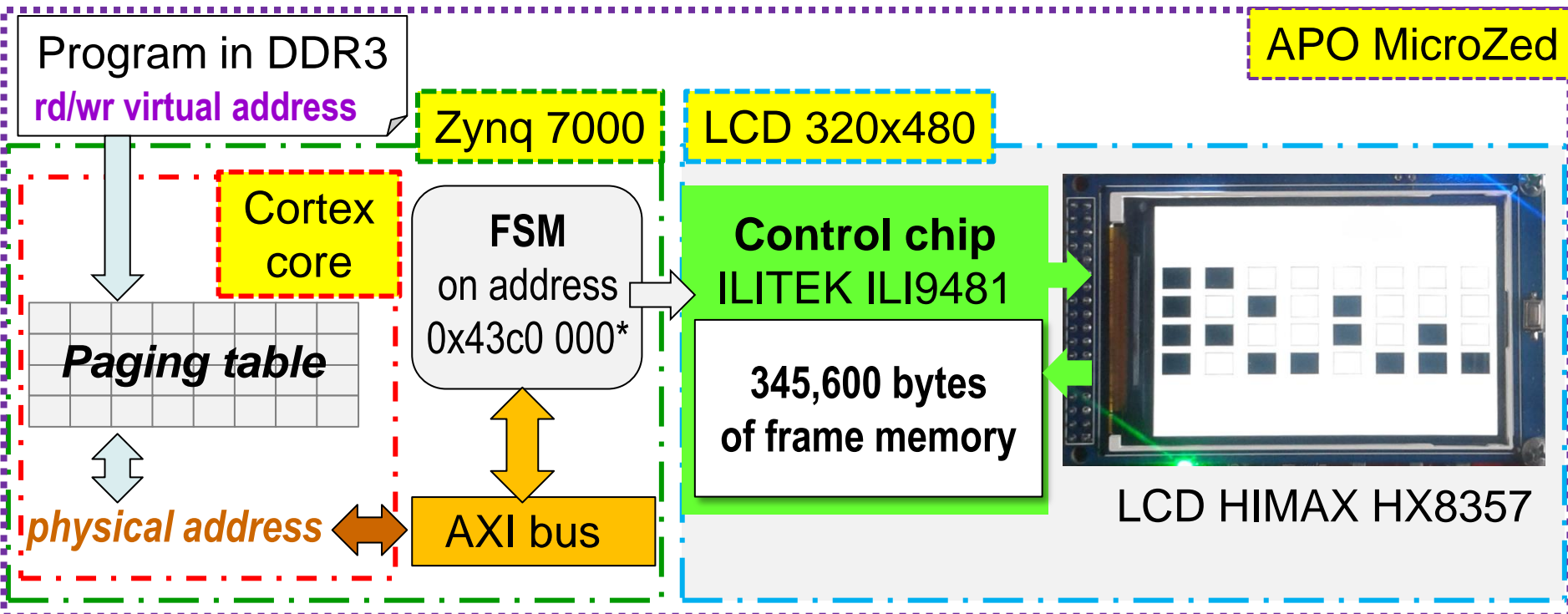
If some address is in range 0x43c0 0000 to 0x43c0 000F then it accepts corresponding data for LCD.



# LCD read/write

FSM transmit data to LCD by generating appropriate signals for LCD control chip that periodically refreshes TFT-LCD display.

If a new request appears before the previous is done, FSM is sending WAIT to AXI bus until it can accept next data/command.



# LCD read/write

Virtual Base Address	Data Type	Control Chip Operation
+0	uint16_t	0x1 - reset LCD, bit0 == 0 - no function
+8	uint16_t	LCD control command
0xC	uint16_t	write 16 bit color pixel (bits 15..0) to frame memory
0xC	uint32_t	write 2 following pixels: bits 15..0   bits 31..0 to mem.

APO MicroZed

Program in DDR3  
rd/wr virtual address

Zynq 7000

LCD 320x480

Cortex  
core



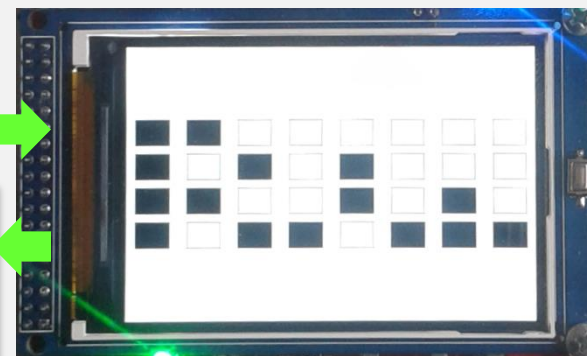
physical address

FSM  
on address  
0x43c0 000\*

AXI bus

Control chip  
ILITEK ILI9481

345,600 bytes  
of frame memory



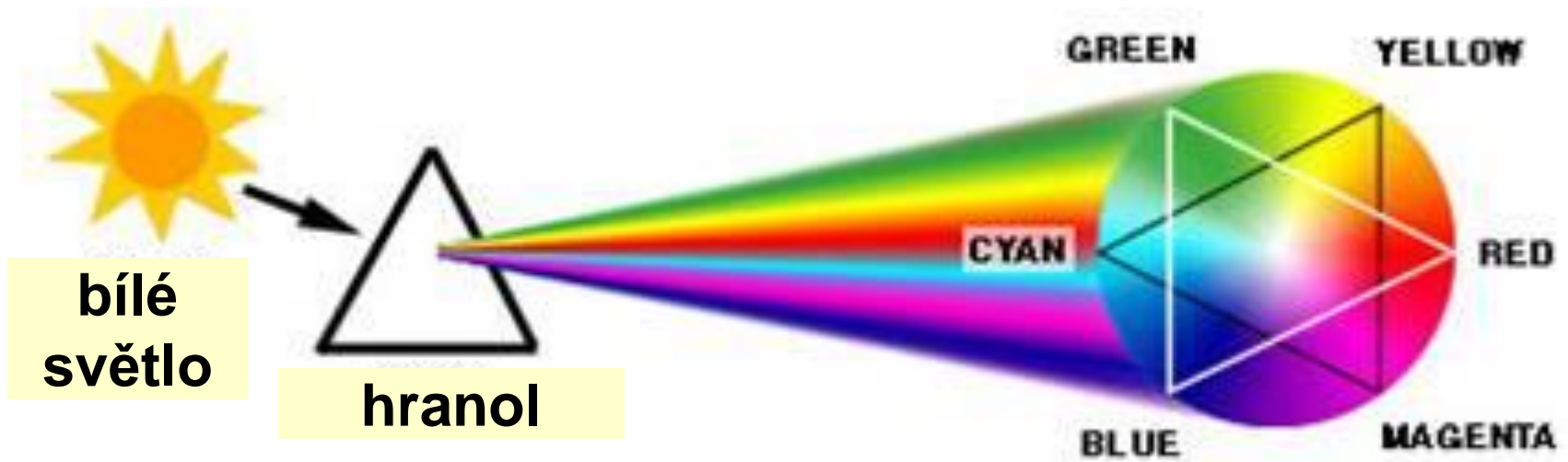
LCD HIMAX HX8357

# *Co je to HSV ?*

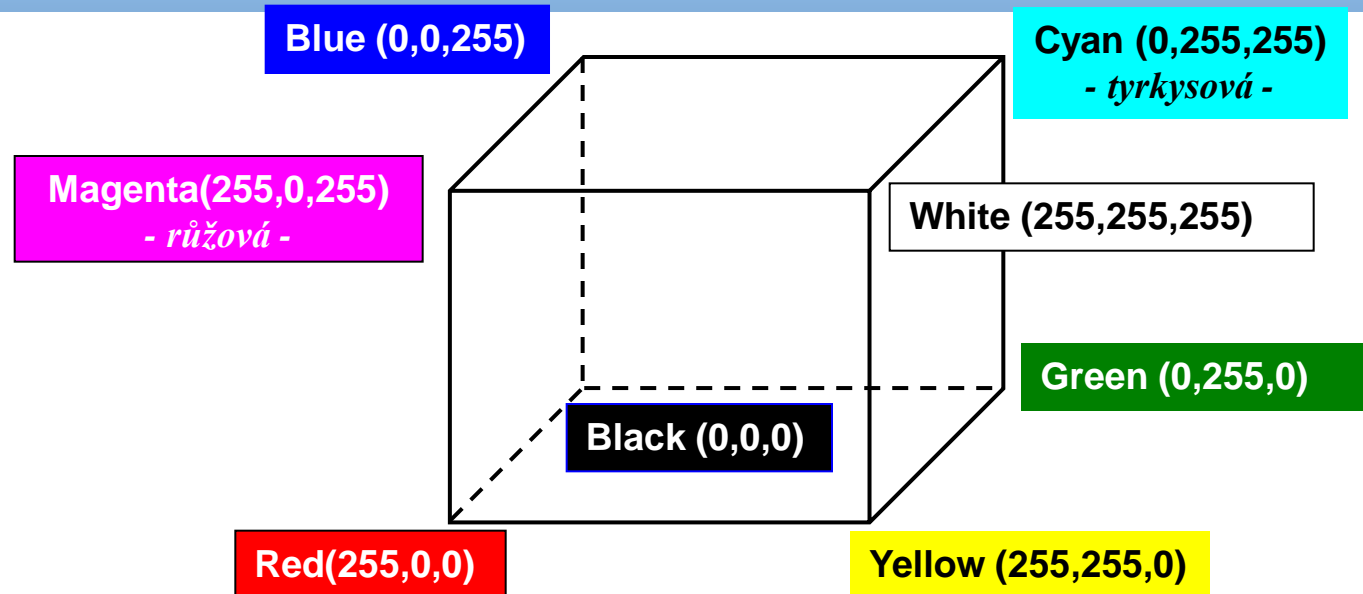
*realita  
versus  
paleta*



# Aditivní míšení barev

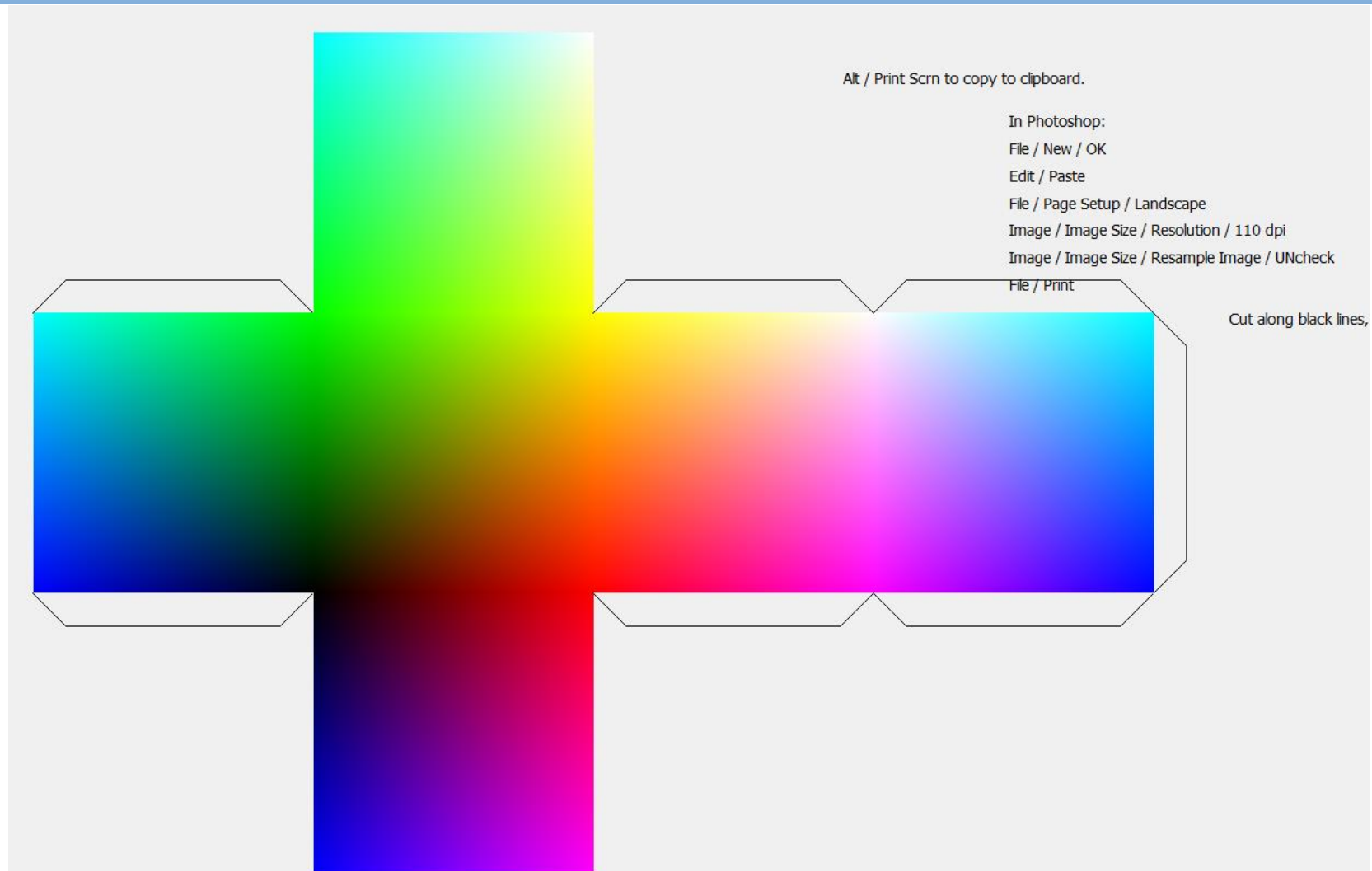


# RGB barevná krychle



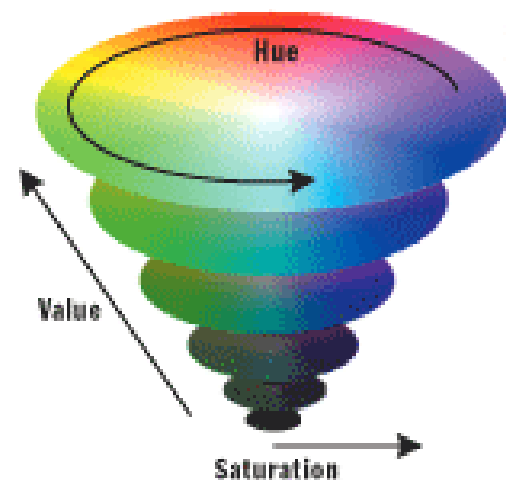
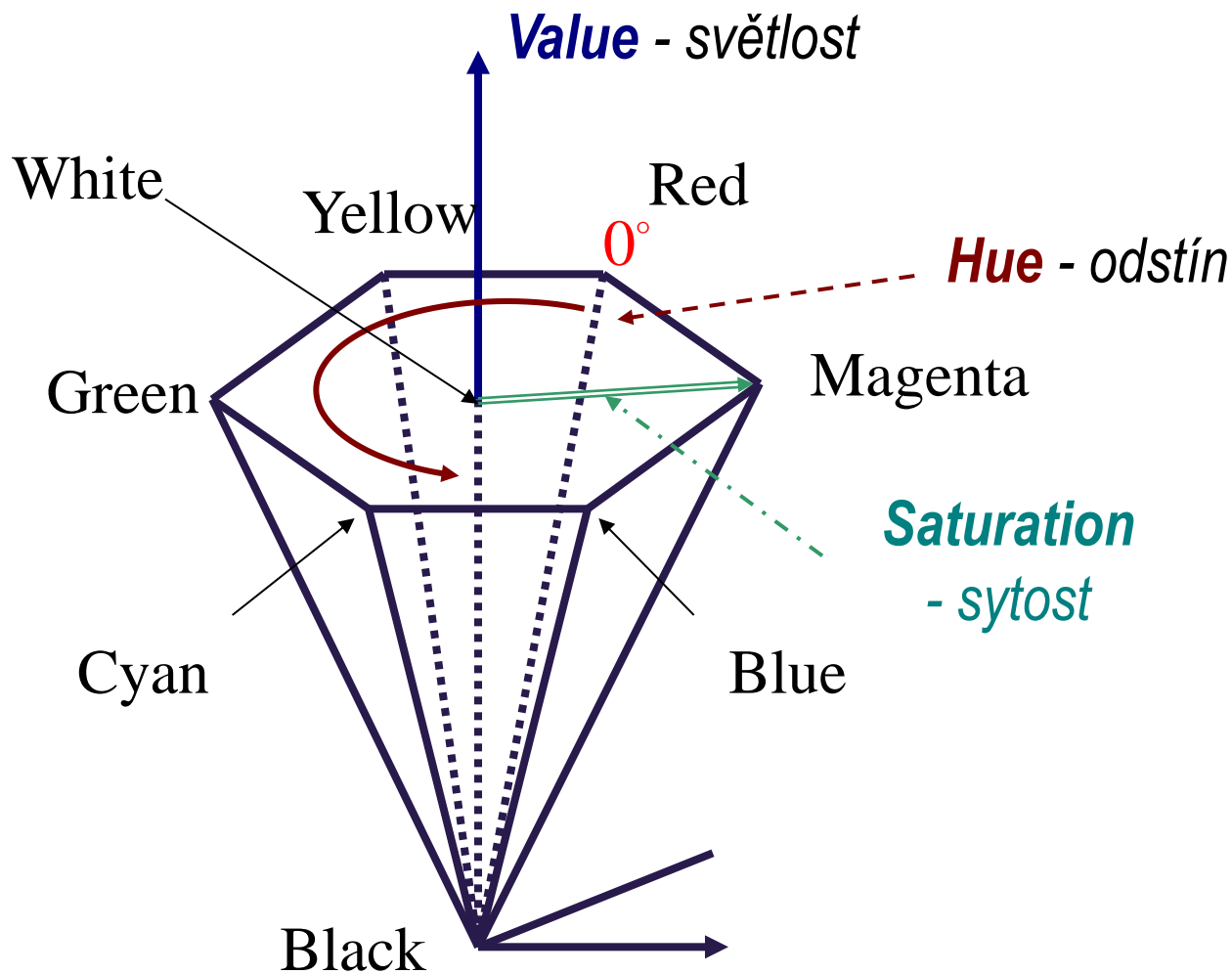
- *Aditivní míchání barev se používá například na monitorech, vlivy jednotlivých barev se sčítají, neboť každá složka se chová jako zdroj světla.*

# RGB Cube with Unintuitive Distribution of Color



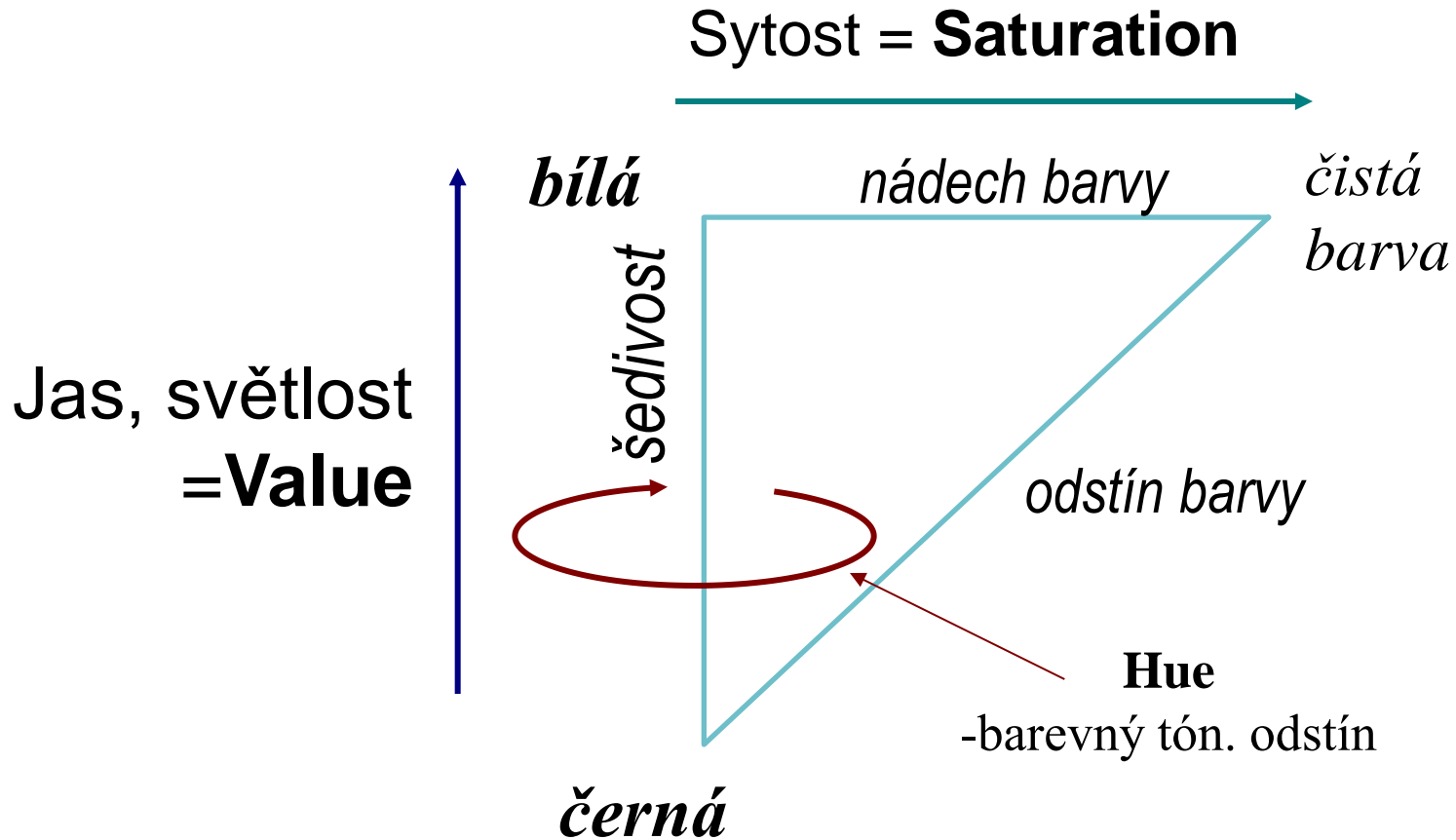
Source: <http://people.duke.edu/~ng46/borland/graphics.htm>

# HSV systém pro intuitivní tvorbu barev



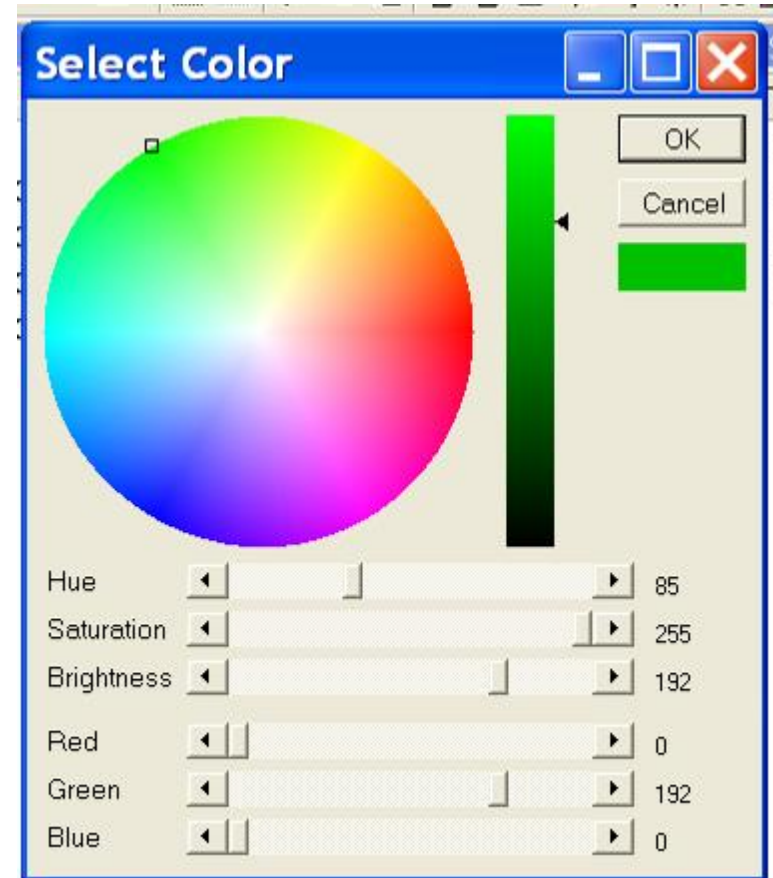


# Význam parametrů HSV



## Example of HSV Color Picker

*Převod mezi RGB a HSV je poměrně složitý, ale existují C kódy na webu.*



## Pro srovnání CMYK

- *Subtraktivní míchání barev se projevuje při tisku - vlivy jednotlivých barvy se odečítají, jelikož každá složka se chová jako filtr bílého světla.*



- *CMY barevnou krychli dostaneme prohozením protilehlých vrcholů RGB krychle, tj- černá ↔ bílá, žlutá ↔ modrá, apod.*

$$\begin{array}{l} \text{Cyan} \\ \text{Magenta} \\ \text{Yellow} \end{array} \begin{bmatrix} C \\ M \\ Y \end{bmatrix} = \begin{bmatrix} 255 \\ 255 \\ 255 \end{bmatrix} - \begin{bmatrix} R \\ G \\ B \end{bmatrix}$$



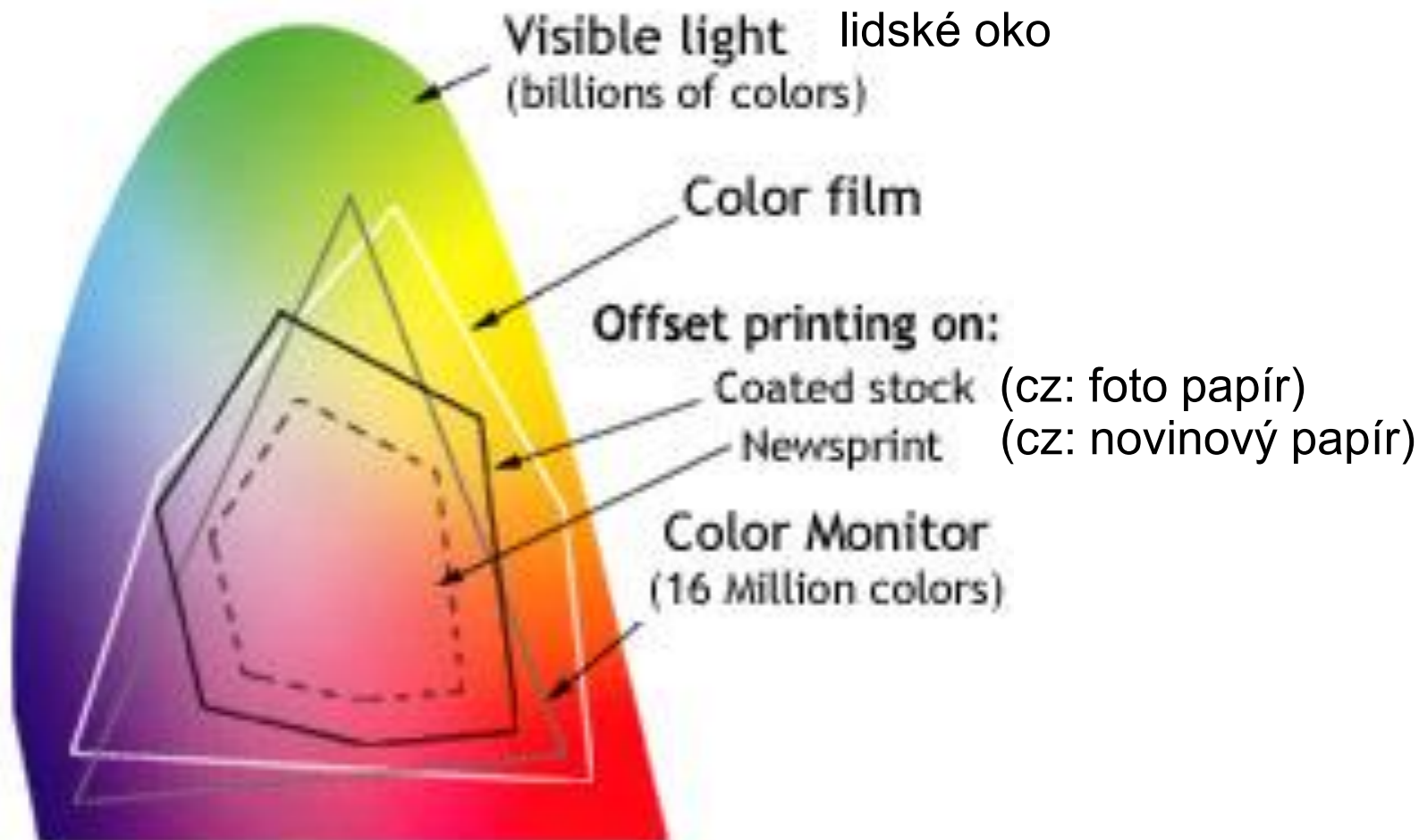
RGB



CMYK

- *Přidáním black dostaneme CMYK:  
 $K = \min(C, M, Y); C = C - K; M = M - K; Y = Y - K;$*

## Získáme ale stejný gamut?



Zdroj: <http://www.kathleenmahoney.com/>

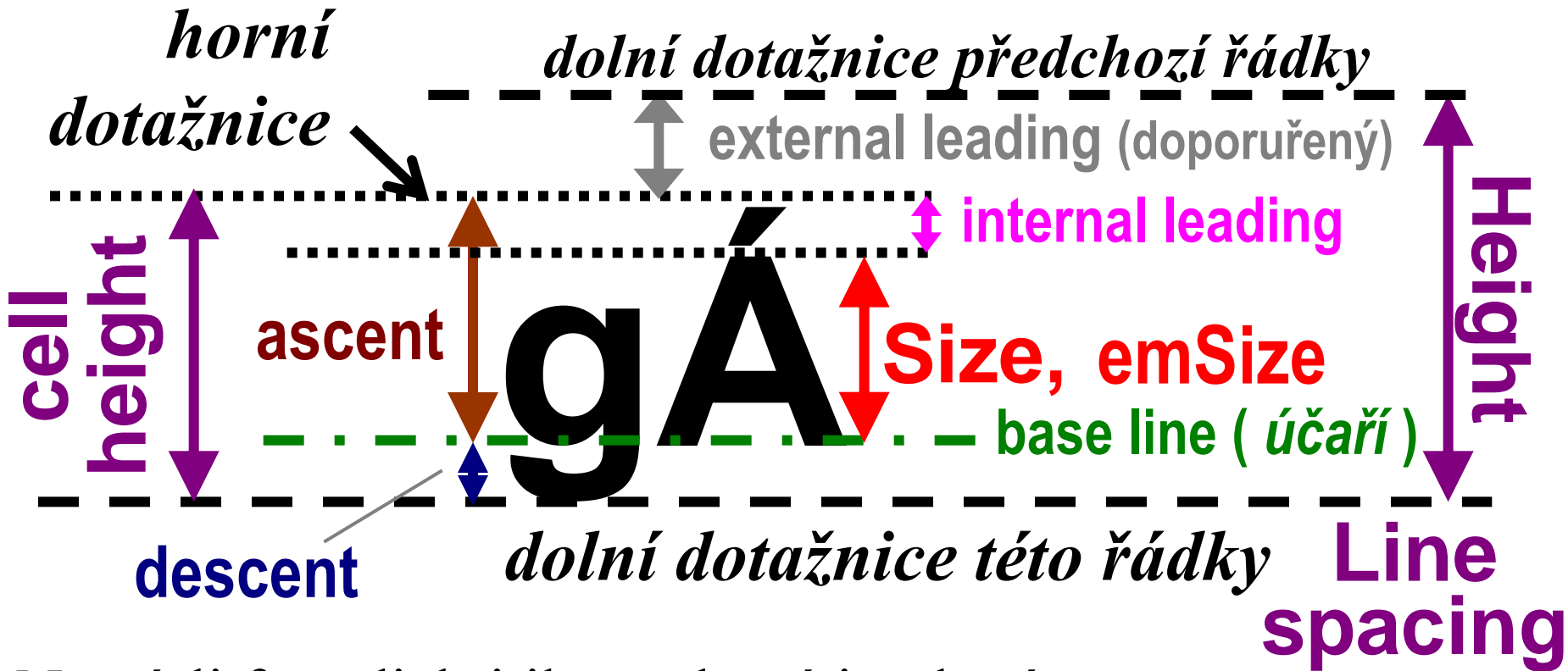
*gamut = rozsah barev zařízení*

# Text to Pixels ?

*LCD has no character generator  
and MicroZed does not contains any graphic card!*



## Velikost fontu



Nemá-li font diakritiku, pak má i nulový internal leading a jeho ascent odpovídá emSize

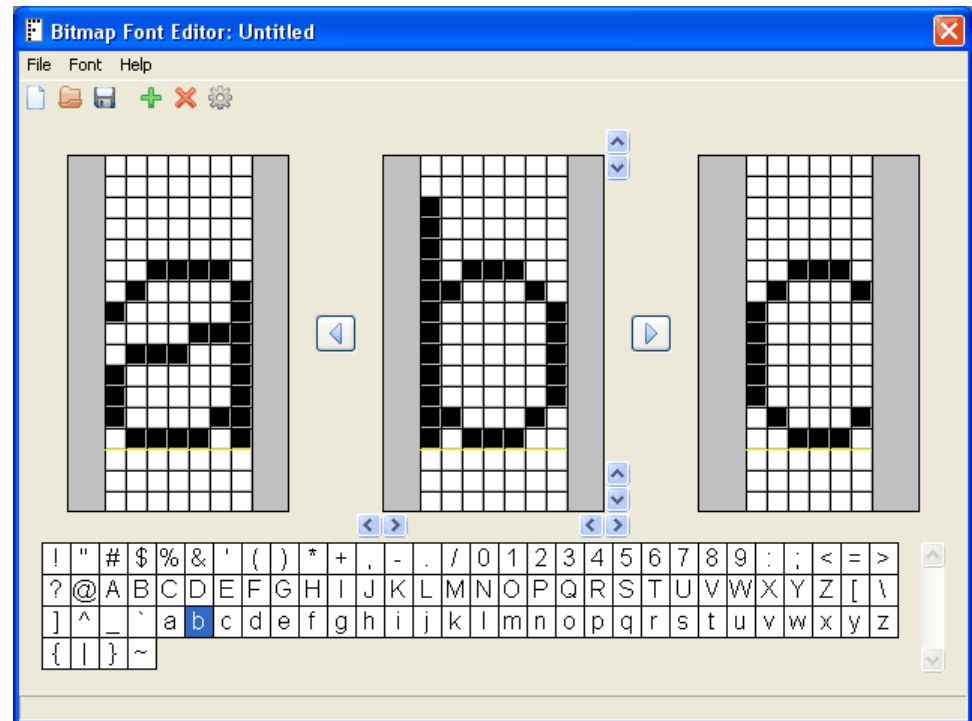
# Bitmap Fonts

Bitmap font are **faster and easier to use** and therefore suitable for low cost computer systems.

<http://growbox.org/doku.php/lcd>

	LOW	HIGH	2	3	4	5	6	7	8	9	A	B	C	D	E	F
			0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
x0	xxxx	0000	0	0	0	0	0	0	0	0	0	0	0	0	0	0
x1	xxxx	0001	!	1	A	Q	a	q	u	a	i					
x2	xxxx	0010	"	2	B	R	b	r	e	A	o					
x3	xxxx	0011	#	3	D	S	s	a	a	o						
x4	xxxx	0100	\$	4	T	T	t	a	o	n						
x5	xxxx	0101	%	5	E	U	e	u	a	o	N					
x6	xxxx	0110	&	6	F	V	f	v	a	o	2					
x7	xxxx	0111	'	7	G	W	w	g	u	o						
x8	xxxx	1000	(	8	H	X	h	x	a	y	z					
x9	xxxx	1001	)	9	I	Y	y	i	e	o	r					
xA	xxxx	1010	*	:	J	Z	j	z	a	u	n					
xB	xxxx	1011	+	;	K	L	k	l	i	k	z					
xC	xxxx	1100	,	<	L	\	l	l	i	e	k					
xD	xxxx	1101	-	=	M	I	m	i	i	#	i					
xE	xxxx	1110	.	>	N	^	n	^	A	B	*					
xF	xxxx	1111	/	?	O	_	o	_	A	f	*					

<http://mobilefonts.sourceforge.net/>



Note: In 1968, the first bitmap font was created by German inventor Rudolf Hell for his Digiset typesetting machine.

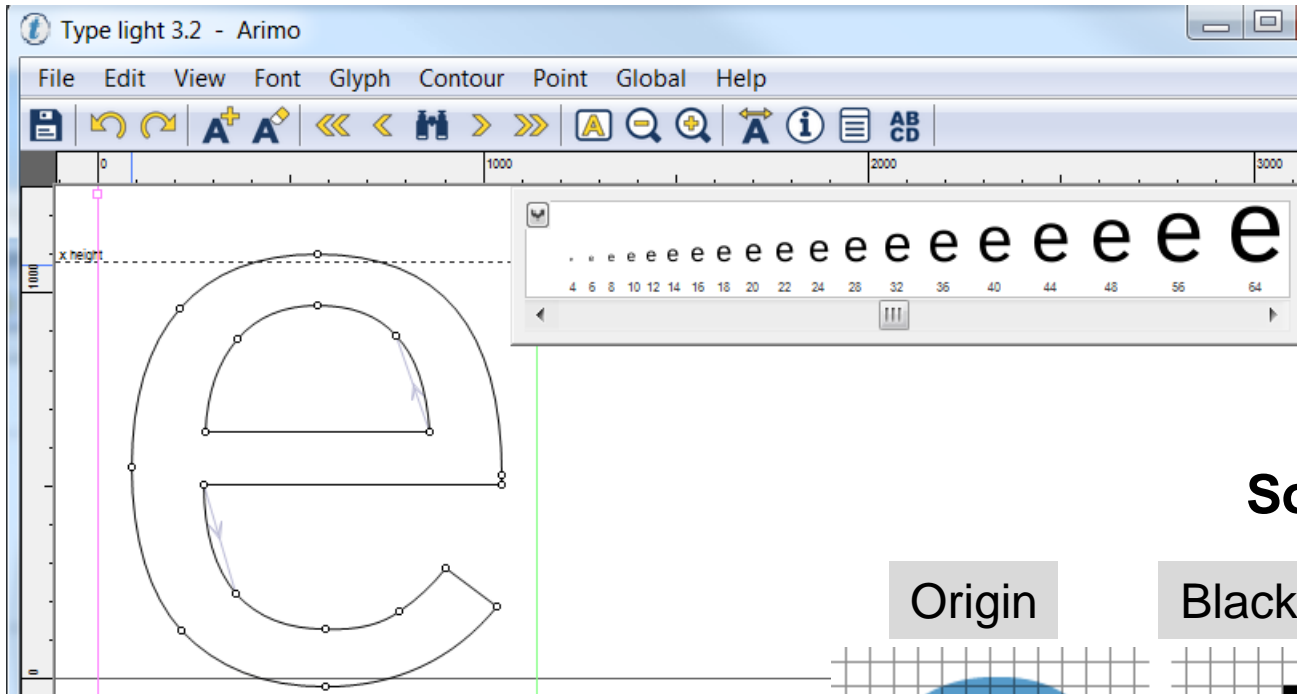
# The Scalable Font Wars

- Apple and Microsoft developed (1980) the **TrueType** methodology that is a system of scalable outline fonts, and can draw characters at low resolution.
- Adobe **PostScript** (1984) is another method of describing an image in terms of *mathematical constructs* (Bézier curves), so it is used not only to describe the individual characters of a font but also to describe entire illustrations and whole pages of text.
- **Open Type** (1996) digital font format was developed jointly by Apple and Microsoft to put an end to the PostScript/TrueType war. Like TrueType, a single file contains all the outline and bitmap data for an OpenType font, but it also contains either PostScript data or additional TrueType data within the font, which in the PostScript case, makes the font truly scalable and exacting.

Source: [wordpress.com](http://wordpress.com)



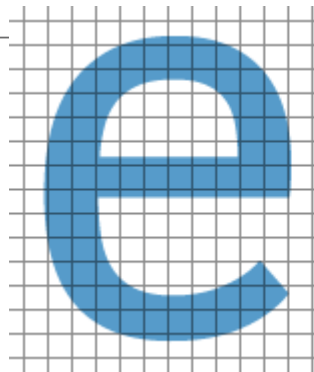
# Rendering of Fonts



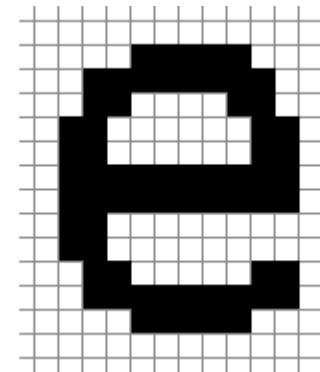
Upper picture:  
program  
[Type Light V3.2](#)

## Some rasterizations

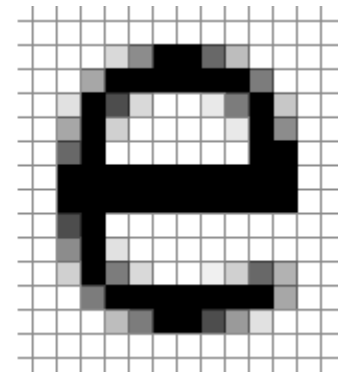
Origin



Black and white



Grayscale



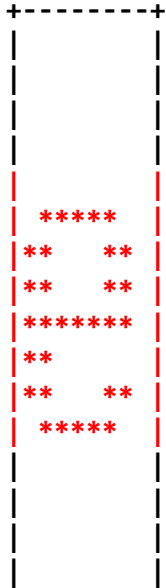
Any scalable font  
must be finally  
rendered (rasterized)  
to pixels of display !

Image source: <https://www.smashingmagazine.com/>

# Black and White Rastered Fonts

```
static font_bits_t rom8x16_bits[] = { ...
/* Character e (0x65):  ht=16, width=8
```

File: font\_rom8x16.c / .h



+-----+ \*/

```
0x0000,0x0000,0x0000,0x0000,
0x0000,
0x7c00,
0xc600,
0xc600,
0xfe00,
0xc000,
0xc600,
0x7c00,
0x0000,0x0000,0x0000,0x0000,
```

		x-column								y-row
		+0	+1	+2	+3	+4	+5	+6	+7	
0x00	0000 0000...									+0
0x00	0000 0000...									+1
0x00	0000 0000...									+2
0x00	0000 0000...									+3
0x00	0000 0000...									+4
0x7c	0111 1100...									+5
0xc6	1100 0110...									+6
0xc6	1100 0110...									+7
0xfe	1111 1110...									+8
0xc0	1100 0000...									+9
0xc6	1100 0110...									+10
0x7c	0111 1100...									+11

# Jak sestavit řídicí program ?



*aneb pozor na paralelní úkony !*

# The Millennium Bridge London



**Slavnostně  
otevřen**

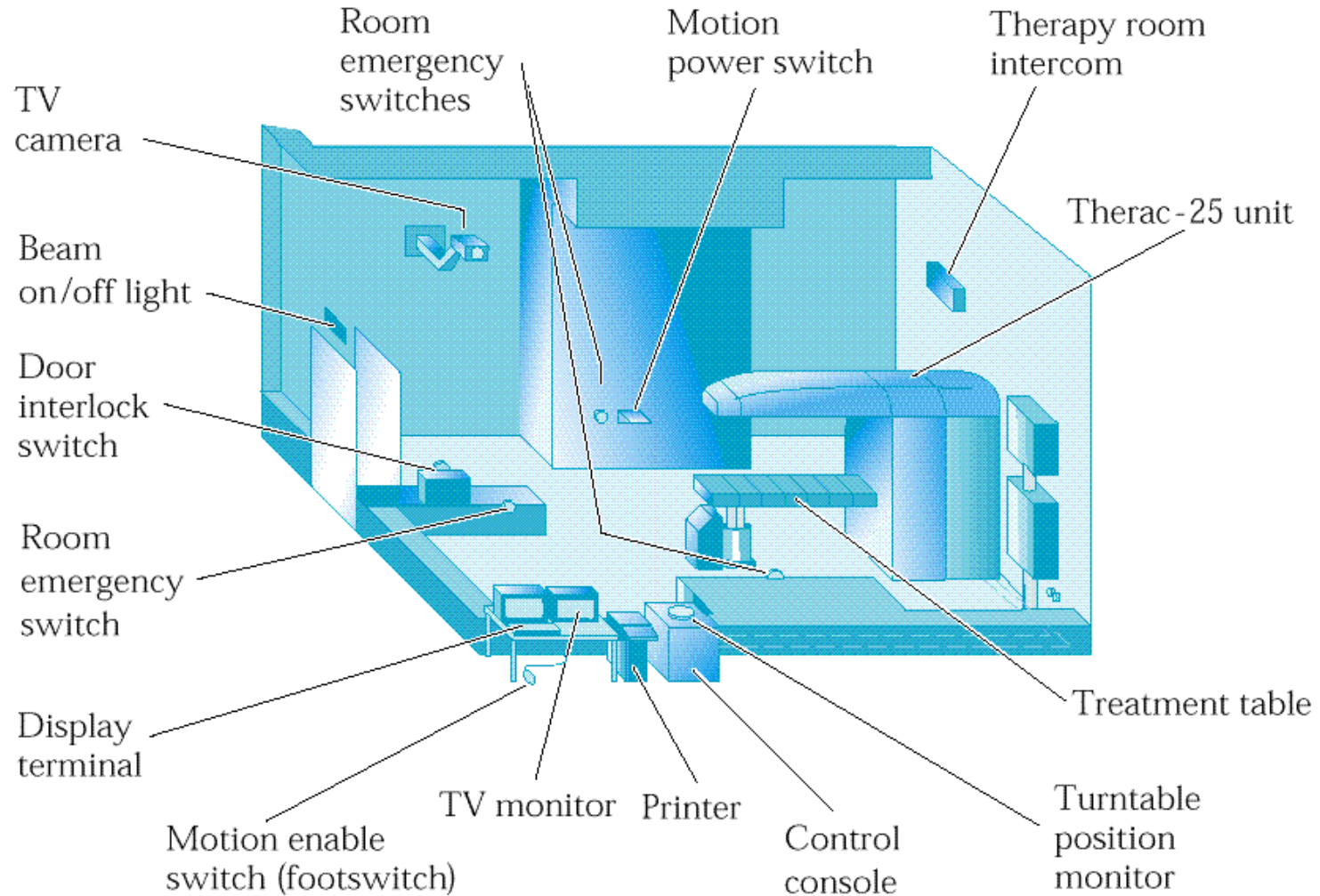
v sobotu  
10.6.2001

**Rychle  
zavřený**

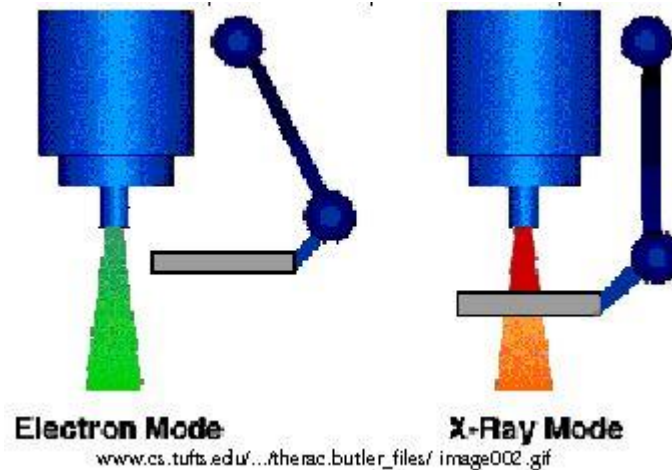
v pondělí  
12.6.2001

*Přímo učebnicový příklad chyby v návrhu*

# Therac 25 – fatální chyba v programu



# Mask of Therac 25



*2 deadly errors escaped detection*

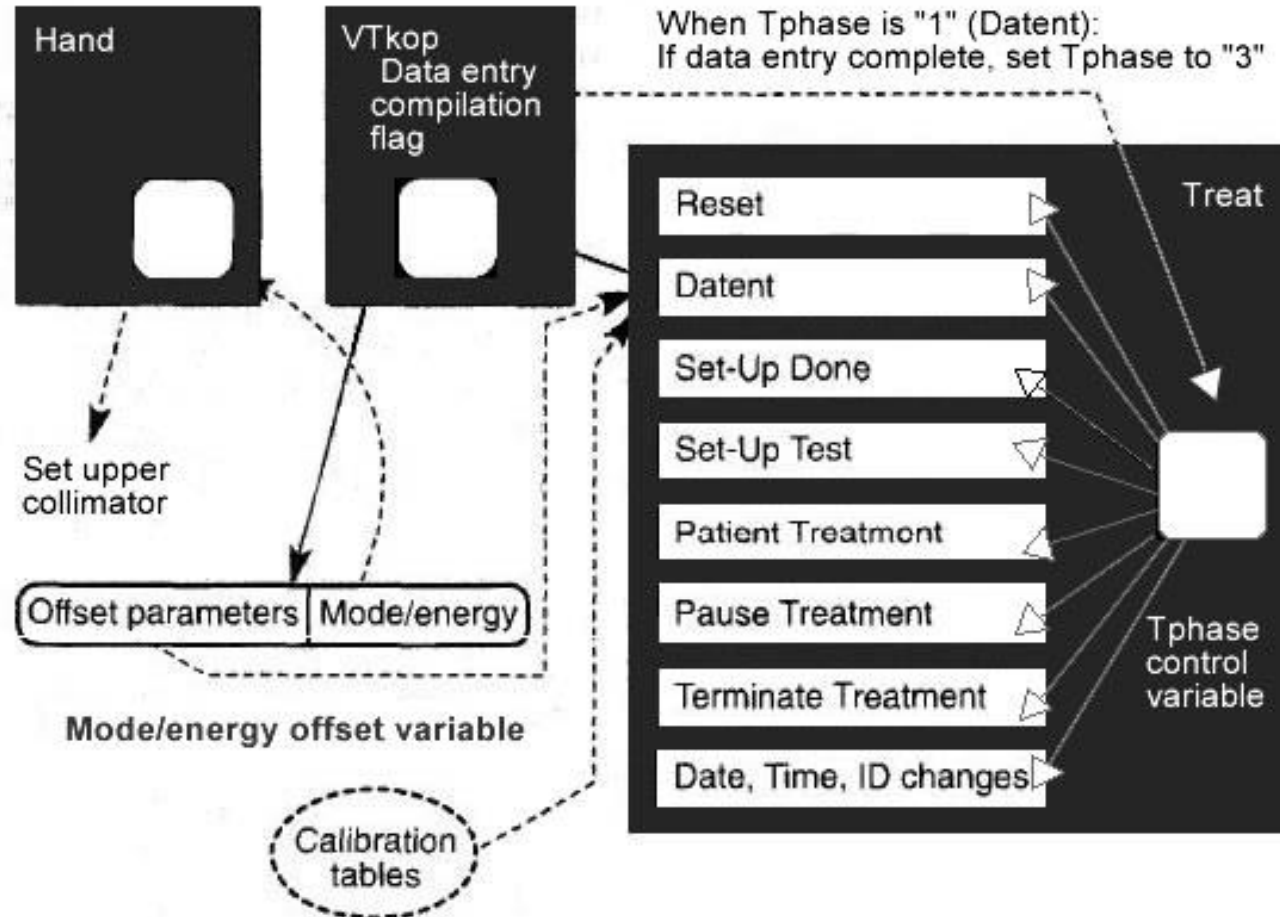
- *during 2 years testing by the manufacture*
    - *during 2 deep inspections*
  - *during deep inspection perform by US government*
- even if all knew what they should look for*



# Operator sidebar

PATIENT NAME : TEST		A	1
TREATMENT MODE: FIX	BEAM TYPE: X ENERGY (KeV):	25	
	ACTUAL	PRESCRIBED	
UNIT RATE/MINUTE	0	200	
MONITOR UNITS	50 50	200	
TIME (MIN)	0.27	1.00	
GANTRY ROTATION (DEG)	0.0	0	VERIFIED
COLLIMATOR ROTATION (DEG)	359.2	359	VERIFIED
COLLIMATOR X (CM)	14.2	14.3	VERIFIED
COLLIMATOR Y (CM)	27.2	27.3	VERIFIED
WEDGE NUMBER	1	1	VERIFIED
ACCESSORY NUMBER	0	0	VERIFIED
DATE : 84-OCT-26	SYSTEM: BEAM READY	OP.MODE: TREAT	AUTO
TIME : 12:55. 8	TREAT : TREAT PAUSE		X-RAY 173777
OPR ID: T25VO2-RO3	REASON: OPERATOR	COMMAND:	

# Structure of code



[source: Nancy G. Leveson, Clark S. Turner, An Investigation of the Therac-25 Accidents]



# 1 of 2 errors

Error is clear only if you know its exact location

Magnet:

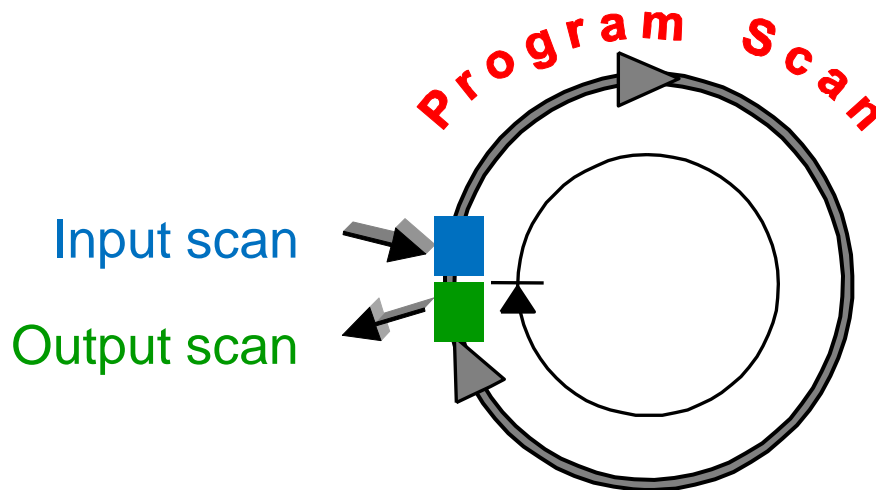
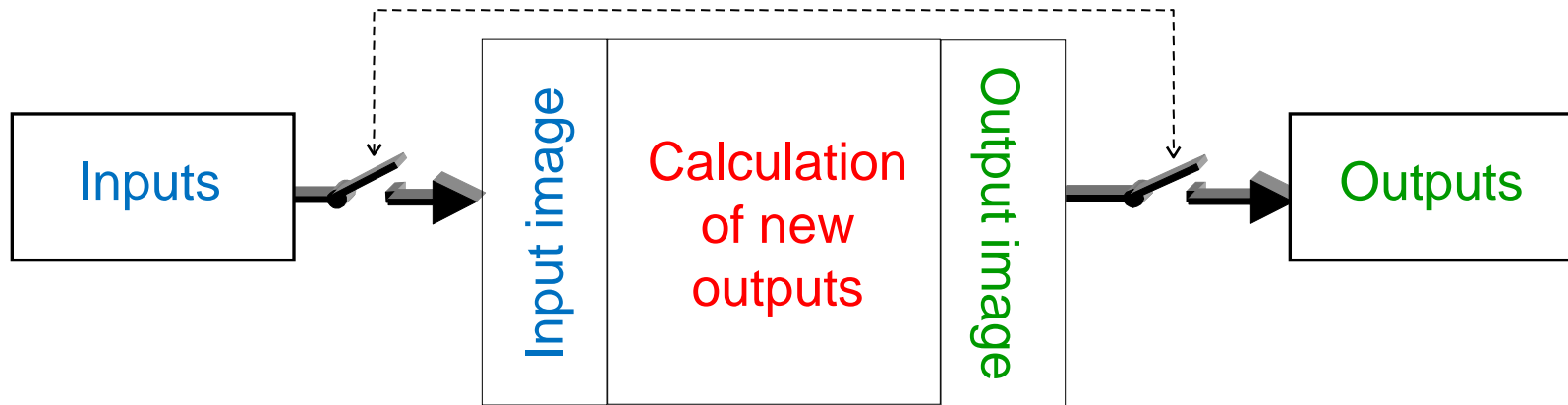
```
Set bending magnet flag           // ..but the flag is reset after 1st call of Ptime
repeat Set next magnet
      Call Ptime
      if mode/energy has changed, then exit
until all magnets are set         // it takes 8 s to adjust magnets!!!
return
```

Ptime:

```
repeat
  if bending magnet flag is set then
    if editing taking place then // it is tested only if bending magnet flag is set
      if mode/energy has changed then exit
until hysteresis delay has expired
Clear bending magnet flag return
```

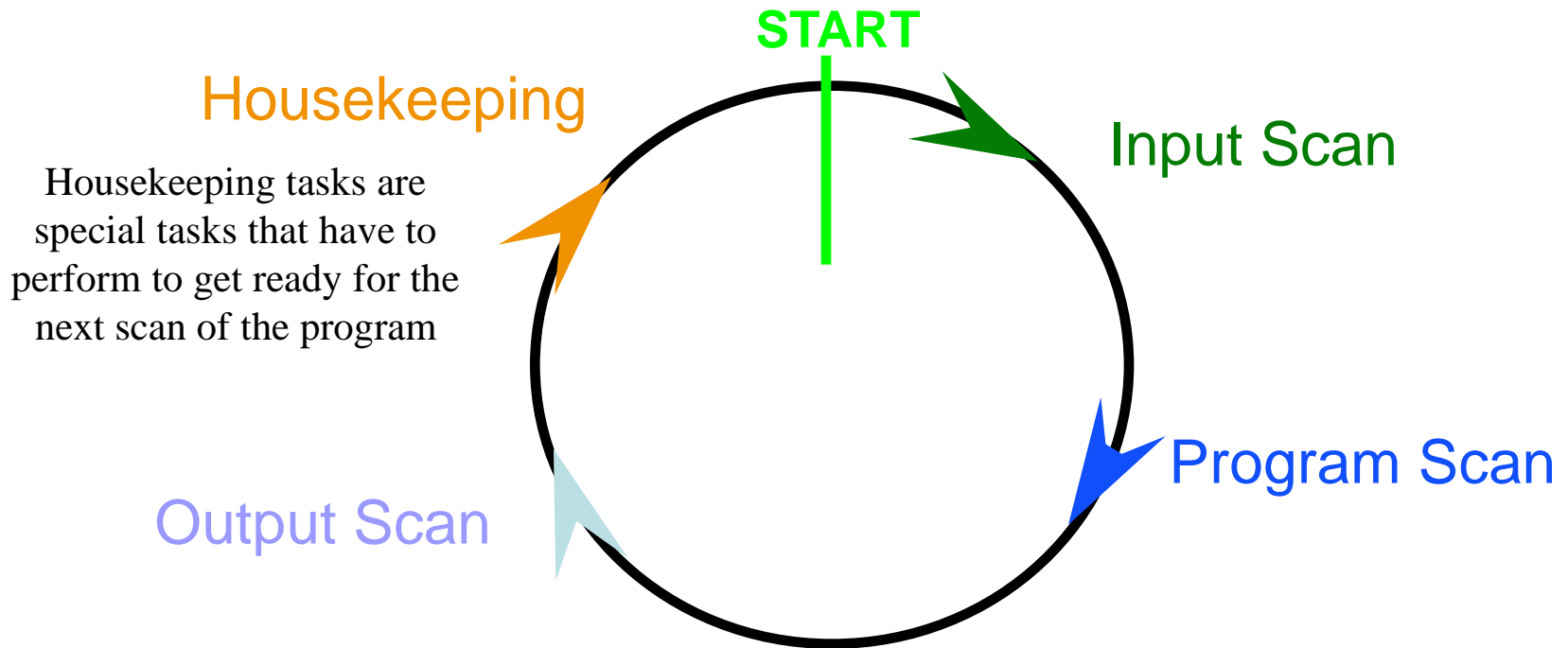
*2nd more complex error appeared when an operator pressed key in the same moment when a byte circular counter overflowed*

# Industrial Control System



```
do  
{ ReadInputs();  
  CalculateOutputs();  
  WriteOutputs();  
}  
while(IsRunOn);
```

# Přesněji Program Scan



# Klasický řídicí program

- Program se vykonává periodicky. Nepřístupuje se v něm k vstupům a výstupům přímo, ale pracuje s obrazy jejich dat, uložených ve dvou pamětech - v obraze vstupů a v obraze výstupů. Vzniká tak periodický cyklus složený ze tří kroků:
  - **Vzorkování vstupů - scan vstupů** (*input scan*) - načtení hodnot vstupů ze vstupních modulů do paměti zvané obraz vstupů (*input image*).
  - **Výpočet programu - scan programu** (*program scan*) - vykonání celého programu, výpočet nových hodnot výstupů a jejich uložení do paměti zvané obraz výstupů (*output image*).
  - **Zápis výstupů - scan výstupů** (*output scan*) - zápis obrazu výstupů do výstupních modulů.