Computer Architectures

Pipelined instruction execution

Hazards, stages balancing, super-scalar systems

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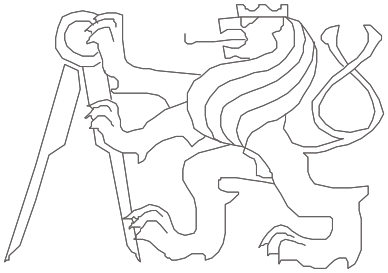
Main source of inspiration: Patterson



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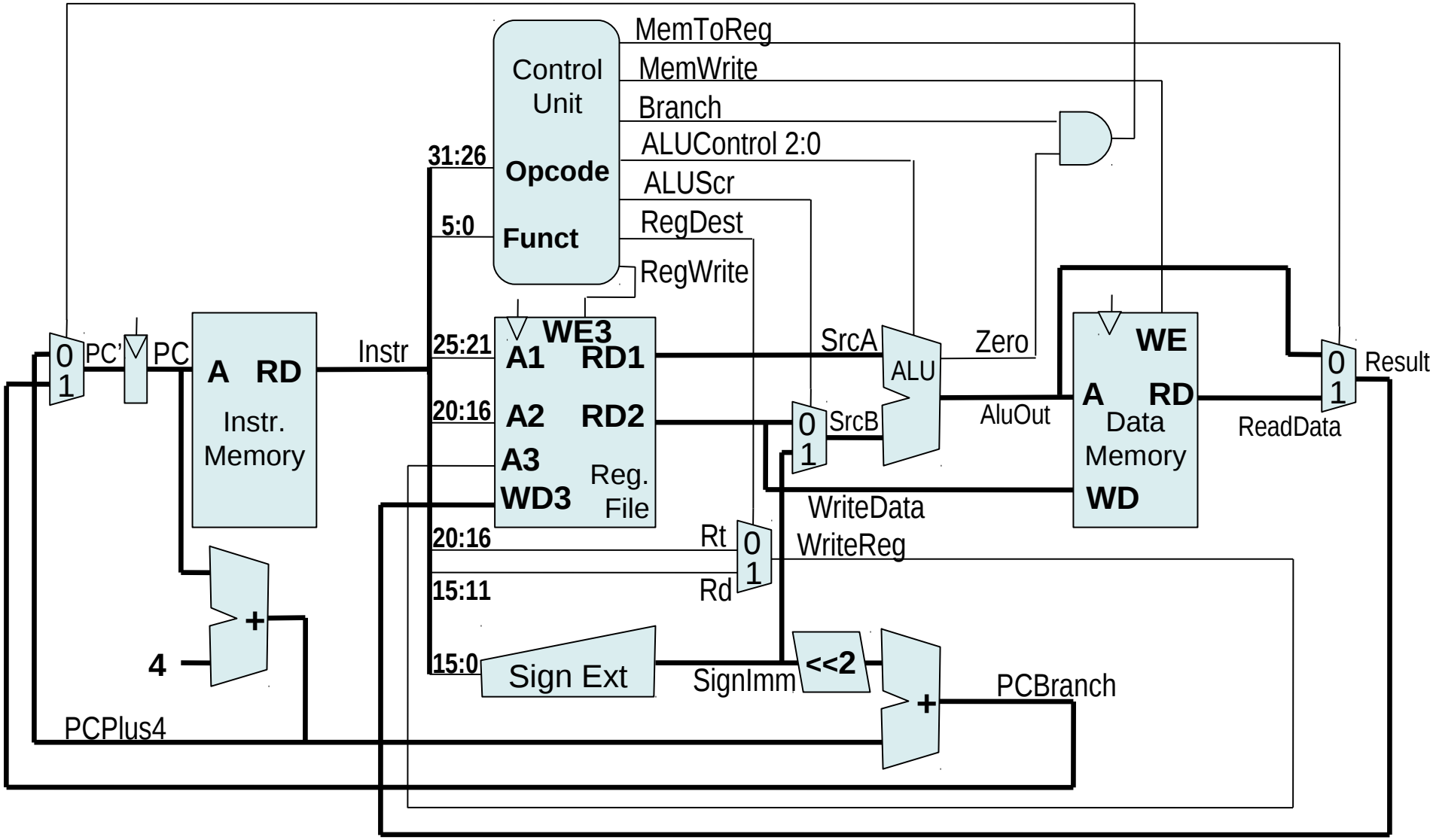
The goal of today lecture

- Convert/extend CPU presented in the lecture 2 to the pipelined CPU design.
- The following instructions are considered for our CPU design:
  `add, sub, and, or, slt, addi, lw, sw` and `beq`

Typ	31…					0
R	**opcode**(6), 31:26	**rs**(5), 25:21	**rt**(5), 20:16	**rd**(5), 15:11	**shamt**(5)	**funct**(6), 5:0
I	**opcode**(6), 31:26	**rs**(5), 25:21	**rt**(5), 20:16	**immediate** (16), 15:0		
J	**opcode**(6), 31:26	**address**(26), 25:0				

Single cycle CPU together with memories

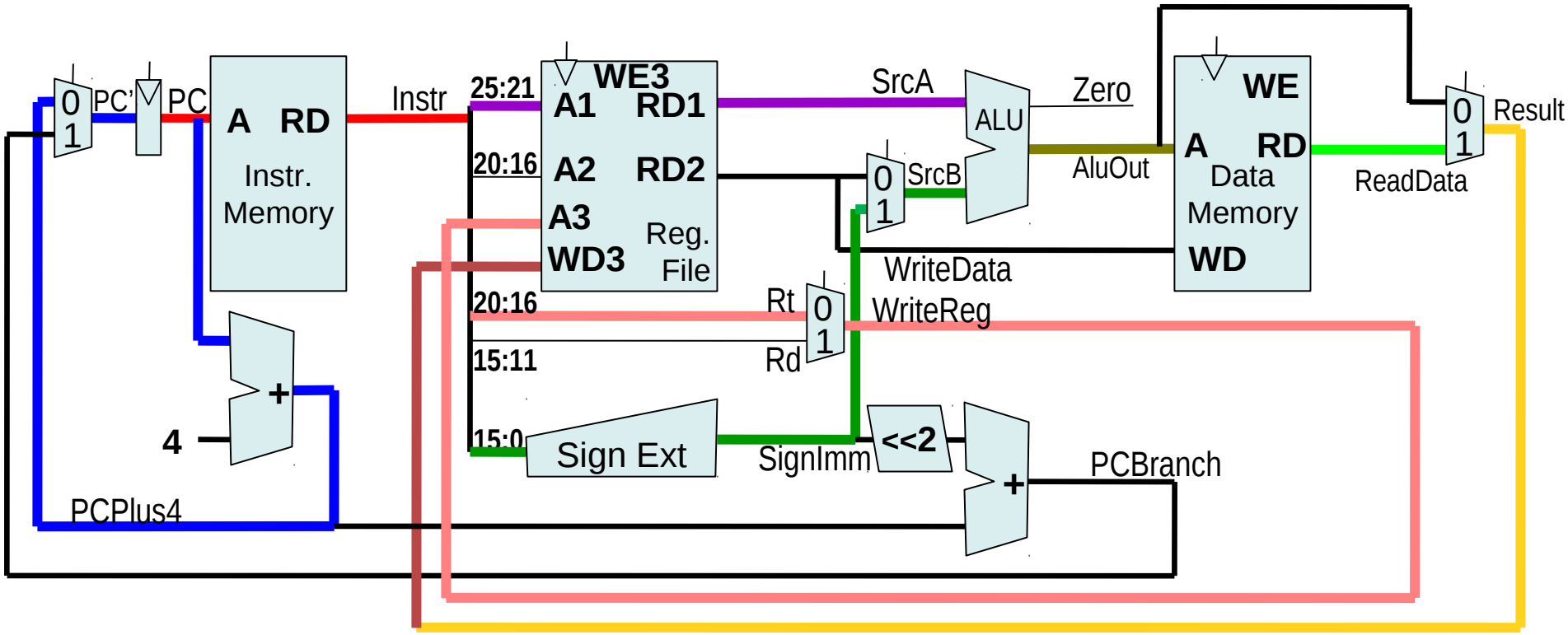


From lecture 2

Single cycle CPU – performance: IPS = IC / T = $IPC_{avg}.f_{CLK}$

- What is the maximal possible frequency of this CPU?
- It is given by latency on the critical path – it is **lw** in our case:

$$T_c = t_{PC} + t_{Mem} + t_{RFread} + t_{ALU} + t_{Mem} + t_{Mux} + t_{RFsetup}$$



From lecture 2

Single cycle CPU – throughput: IPS = IC / T = $IPC_{avg}.f_{CLK}$

- $Tc = t_{PC} + t_{Mem} + t_{RFread} + t_{ALU} + t_{Mem} + t_{Mux} + t_{RFsetup}$
- Consider following parameters

  t_{PC} = 30 ns

  t_{Mem} = 300 ns

  t_{RFread} = 150 ns

  t_{ALU} = 200 ns

  t_{Mux} = 20 ns

  $t_{RFsetup}$ = 20 ns

  Then Tc = 1020 ns --> $f_{CLK\ max}$ = 980 kHz,

  IPS = 1 • 980e3 = 980 000 instructions per second

From lecture 2

Pipelined instructions execution

Suppose that instruction execution can be divided into 5 stages:

IF – Instruction Fetch, ID – Instruction decode (and Operands Fetch),
EX – Execute, MEM – Memory Access, WB – Write Back

and $\tau = \max \{ \tau_i \}_{i=1}^{k}$, where τ_i is time required for signal propagation (*propagation delay)* through *i*-th stage.

IF – setup PC for memory and fetch pointed instruction. Update PC = PC+4

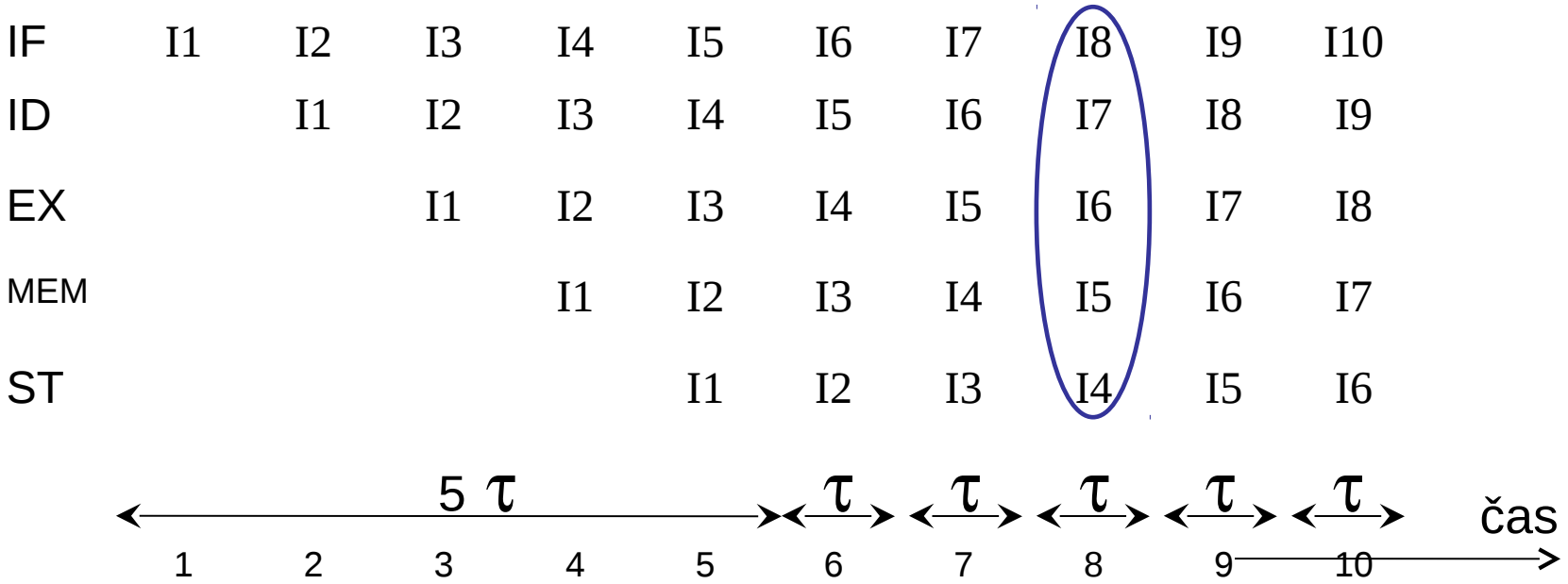
ID – decode the opcode and read registers specified by instruction, check for equality (for possible `beq` instruction), sign extend offset, compute branch target address for branch case (this is means to extend offset and add PC)

EX – execute function/pass register values through ALU

MEM – read/write main memory for *load/store* instruction case

WB – write result into RF for instructions of register-register class or instruction *load* (result source is ALU or memory)

Instruction-level parallelism - pipelining



- The time to execute *n* instructions in the *k*-stage pipeline:

$$T_k = k.\tau + (n-1)\,\tau$$

- Speedup:

$$S_k = \frac{T_1}{T_k} = \frac{nk\,\tau}{k\tau + (n-1)\tau} \qquad \lim_{n \to \infty} S_k = k$$

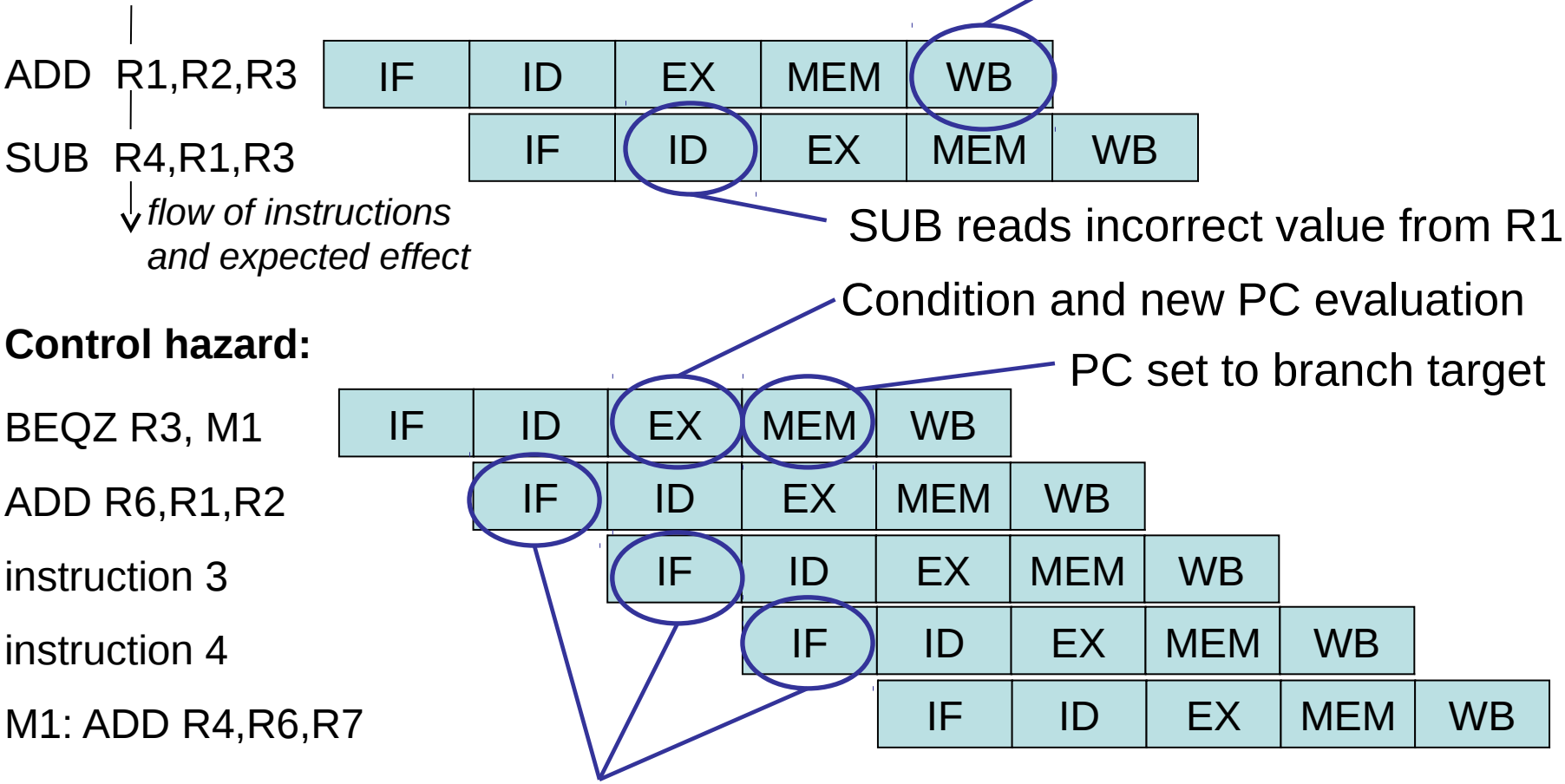
Prerequisite: pipeline is optimally balanced, circuit can arbitrarily divided

Instruction-level parallelism - pipelining

- Does not reduce the execution time of individual instructions, effect is just the opposite...
- Hazards:
  - structural (resolved by duplication),
  - data (result of data dependencies: RAW, WAR, WAW)
  - control (caused by instructions which change PC)...
- Hazard prevention can result in pipeline stall or pipeline flush
- Remark : Deeper pipeline (more stages) results in shorter sequences of gates in each stage which enables to increase the operating frequency of the processor…, but more stages means higher overhead (demand to arrange better instructions into pipeline and result in more significant lag in the case of stall or pipeline flush)

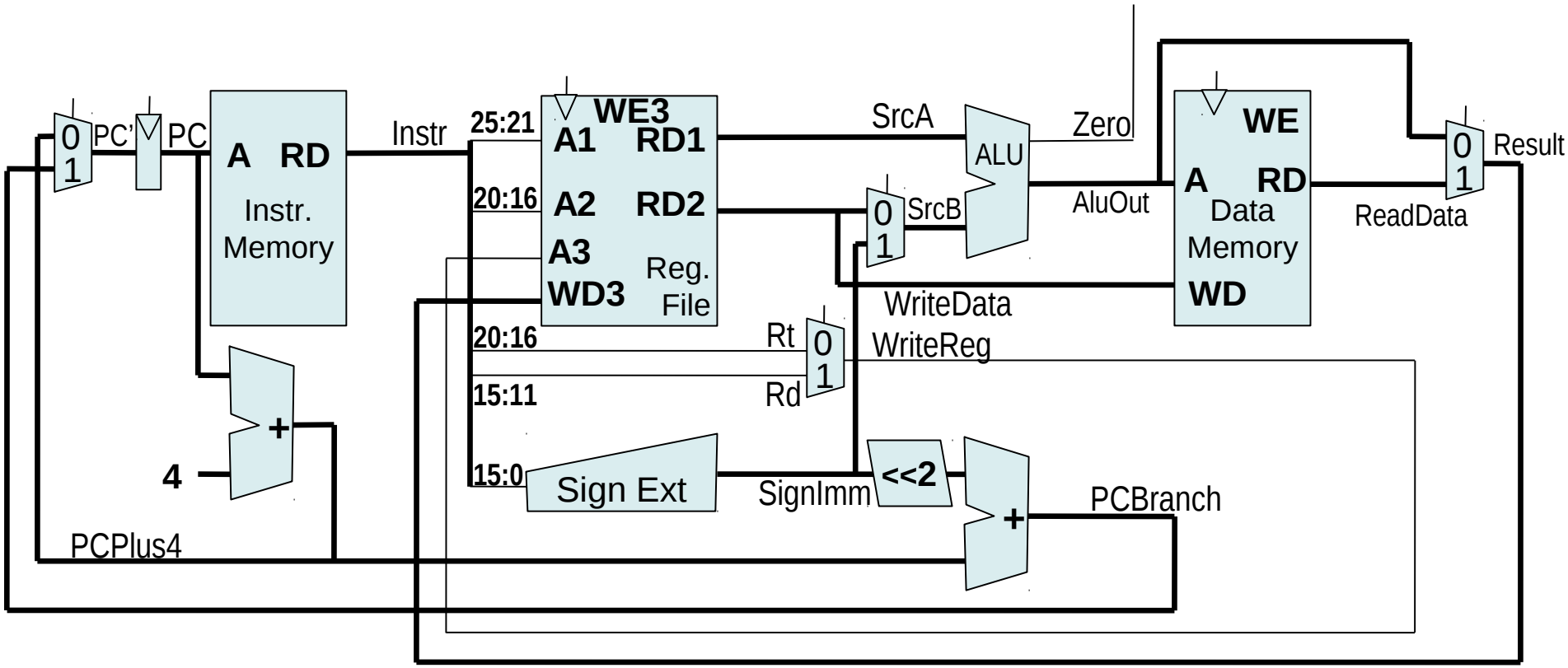
Instruction-level parallelism – Semantics violations

Data hazard:



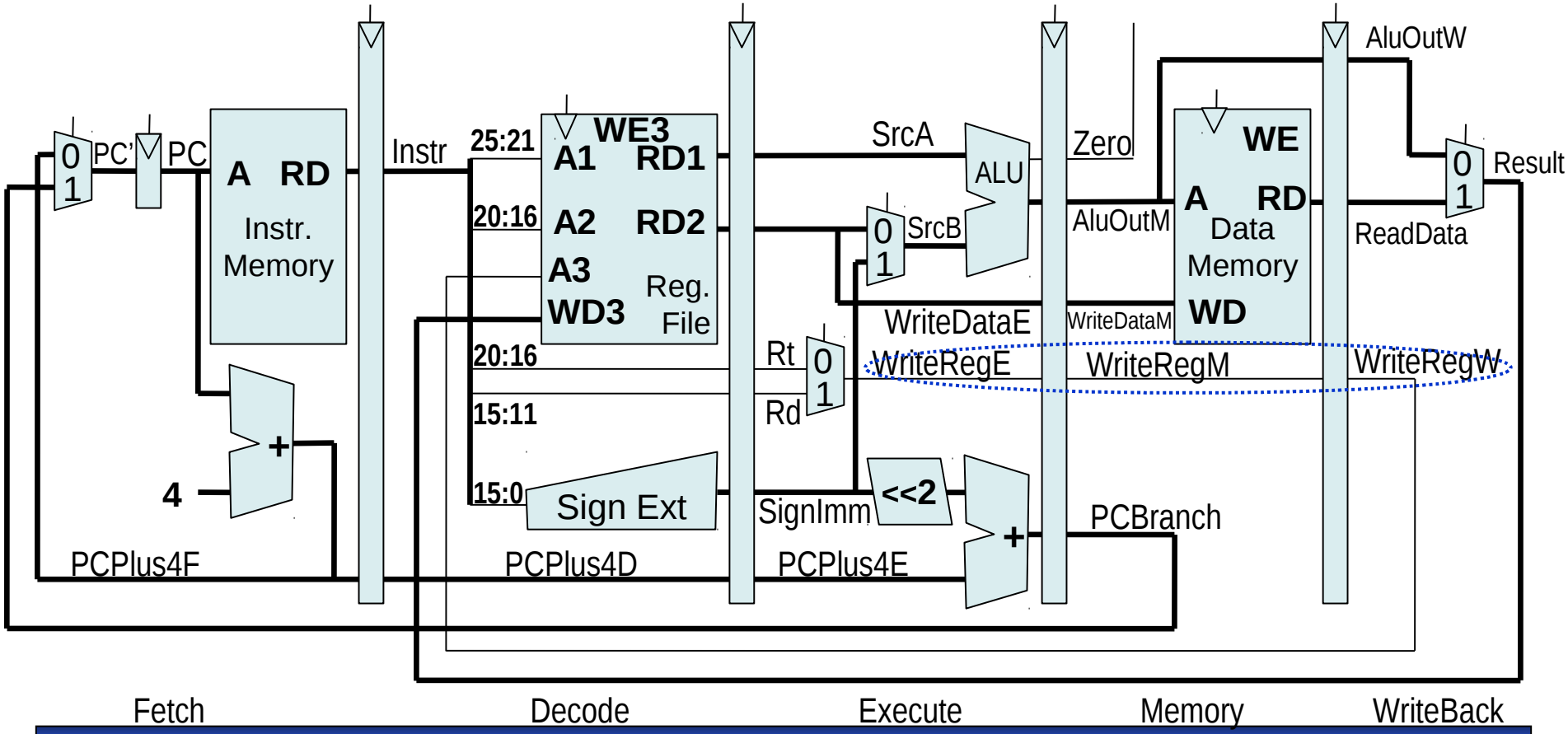
Should be these instructions fetched (and executed then)?

Non-pipelined execution

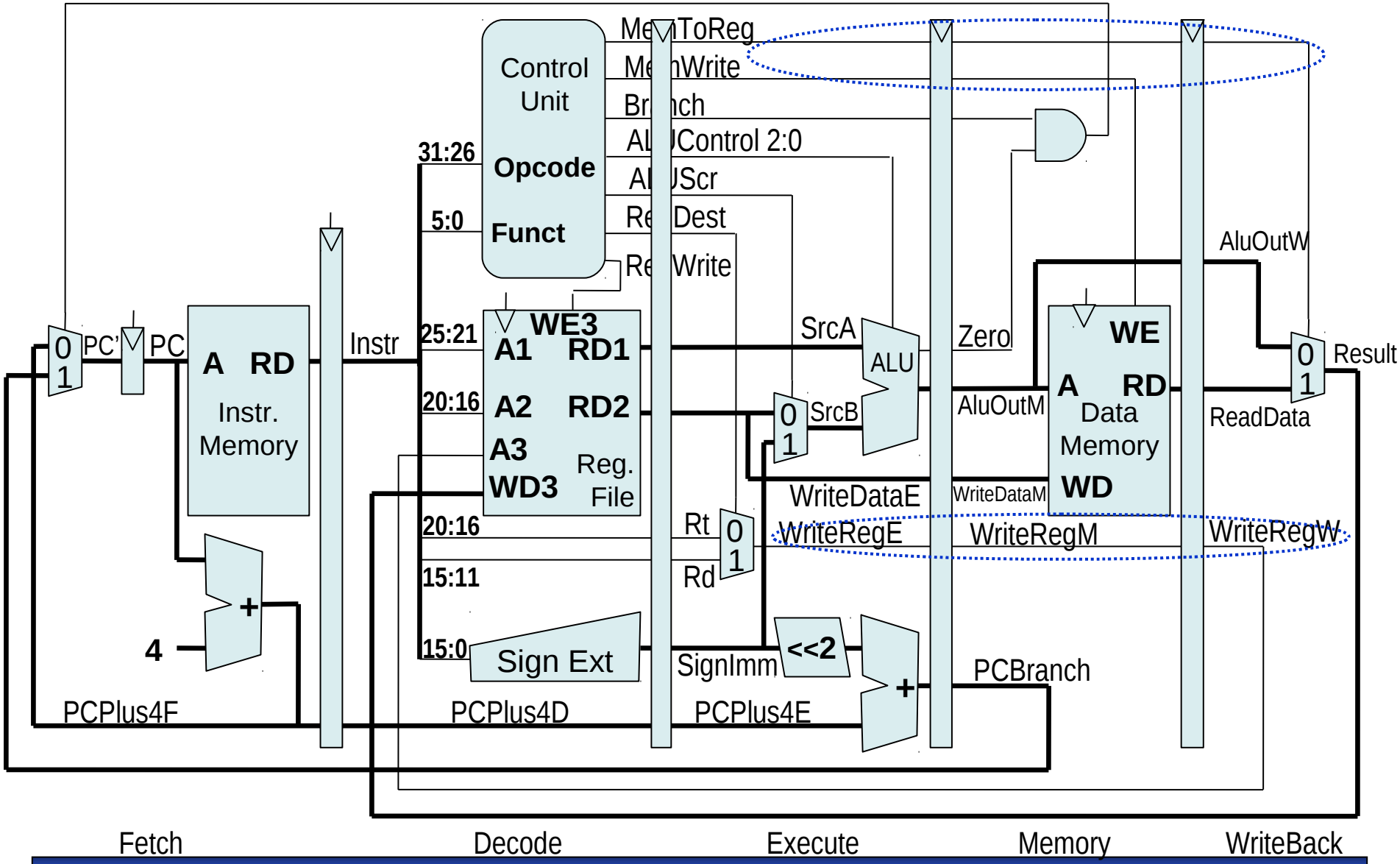


From lecture 2

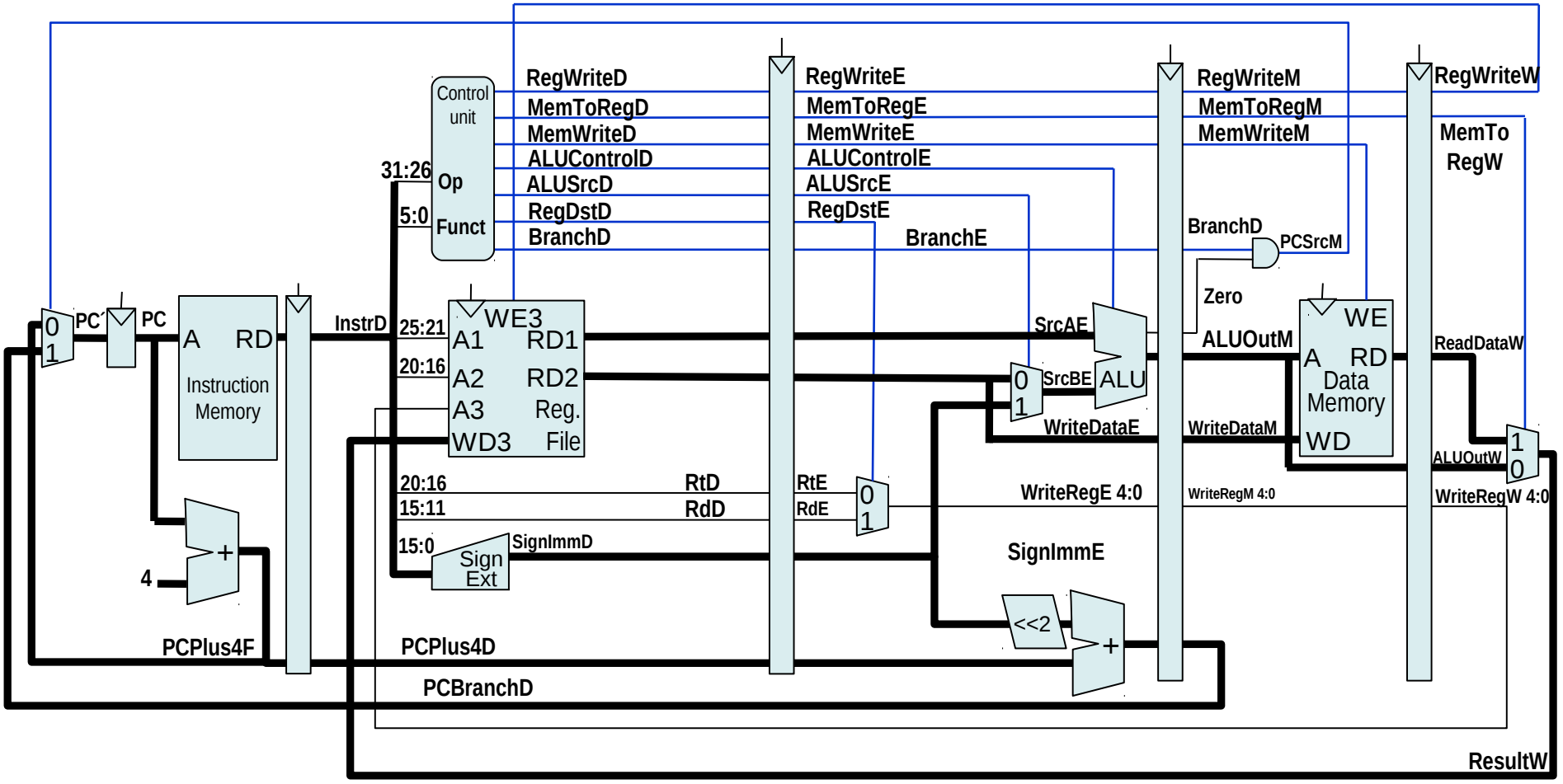
Pipelined execution



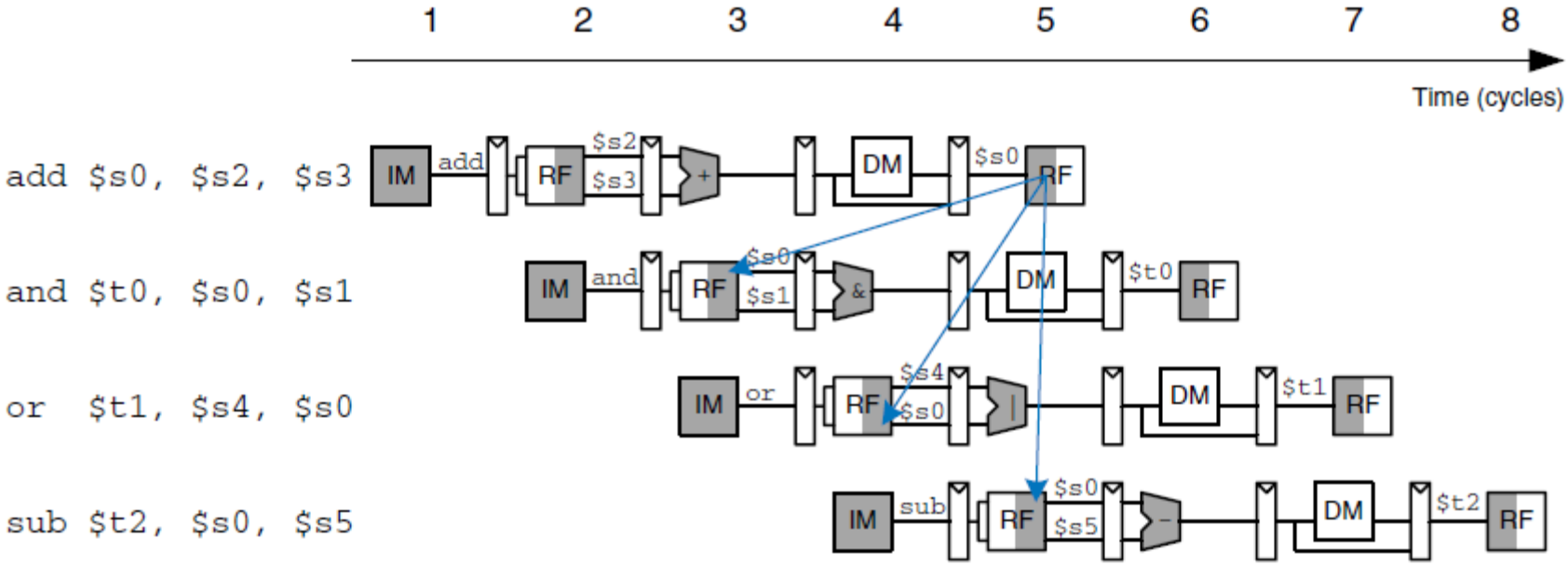
Pipelined execution



The same design but drawn scaled down…

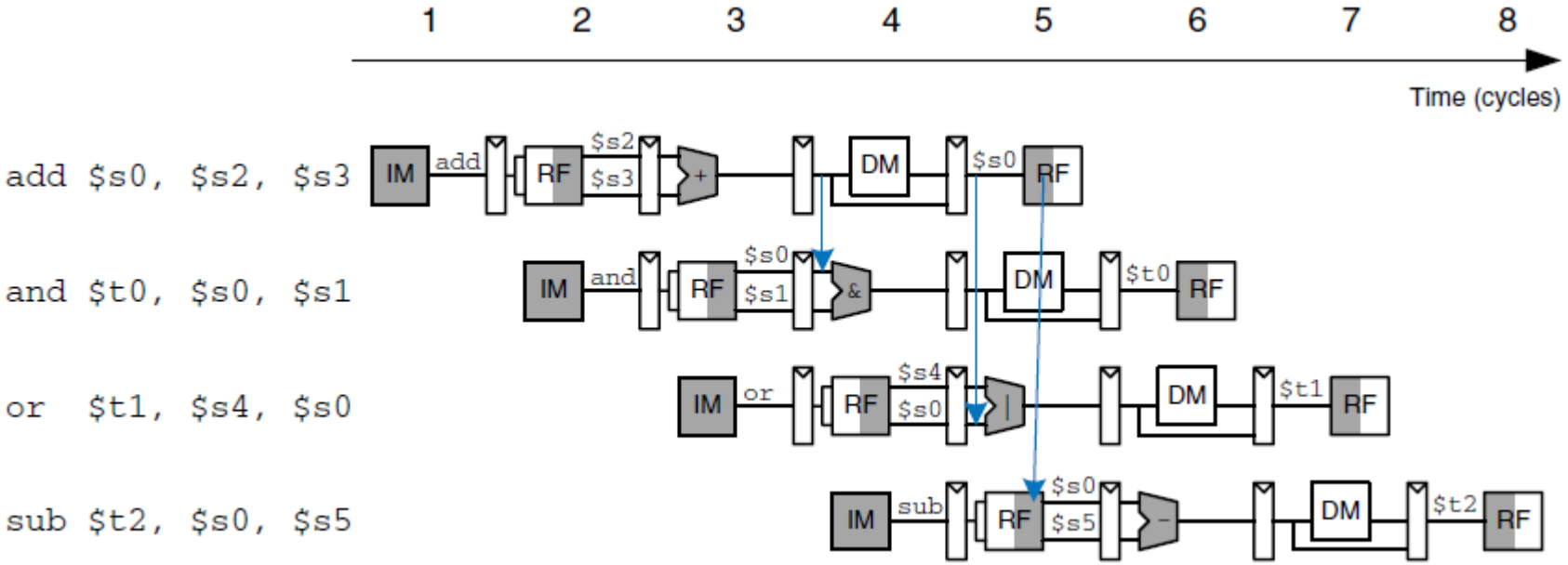


Cause of the data hazards



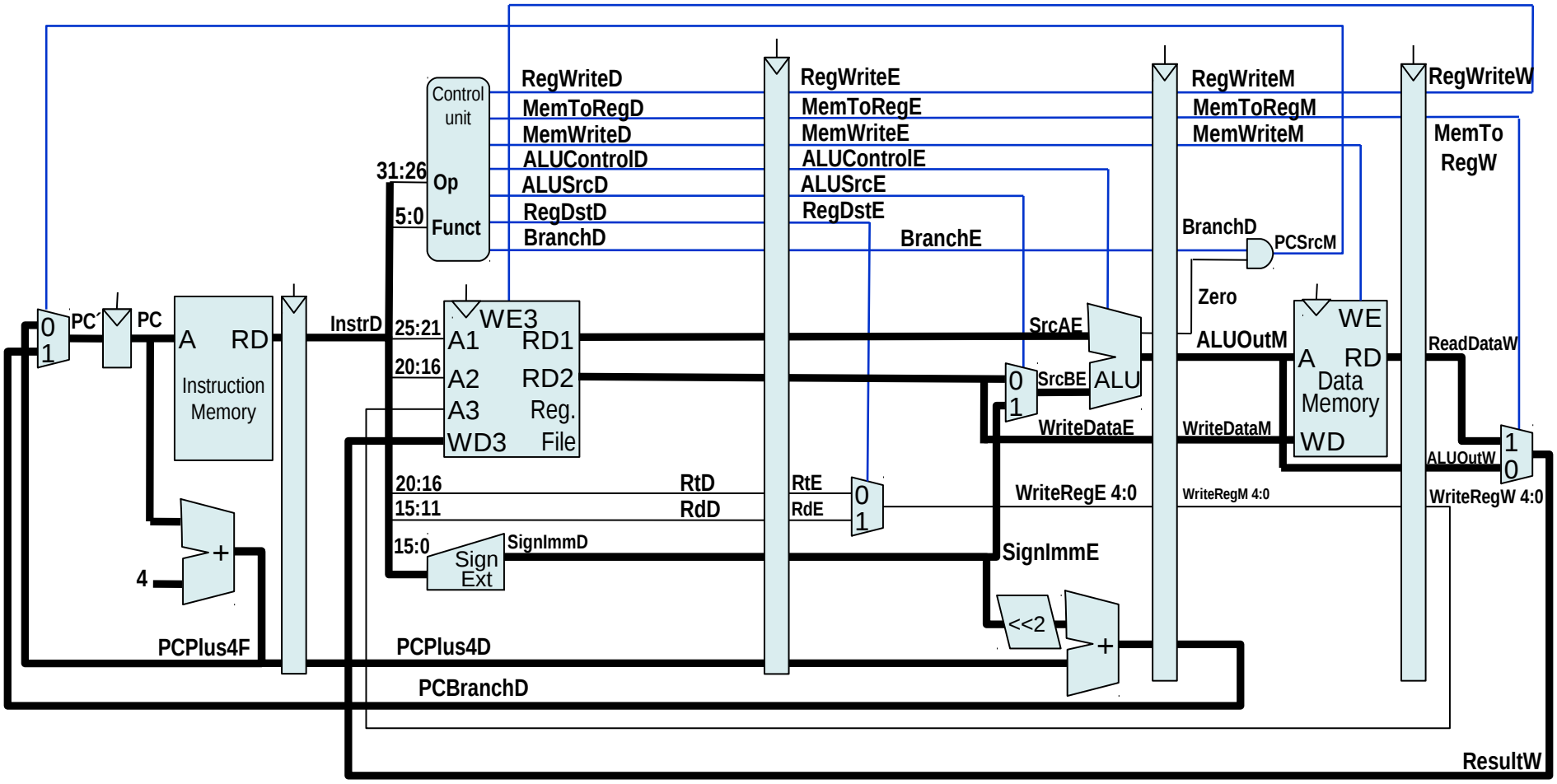
- Register File – access from two pipeline stages (Decode, WriteBack) – actual write occurs at the first half of the clock cycle, the read in the second half ⇒ there is no hazard for `sub $s0` input operand
- RAW (Read After Write) hazard – `and` (`or`) requires `$s0` in 3 (4)
- How can such hazard be prevented without pipeline throughput degradation?

Forwarding to avoid data hazards

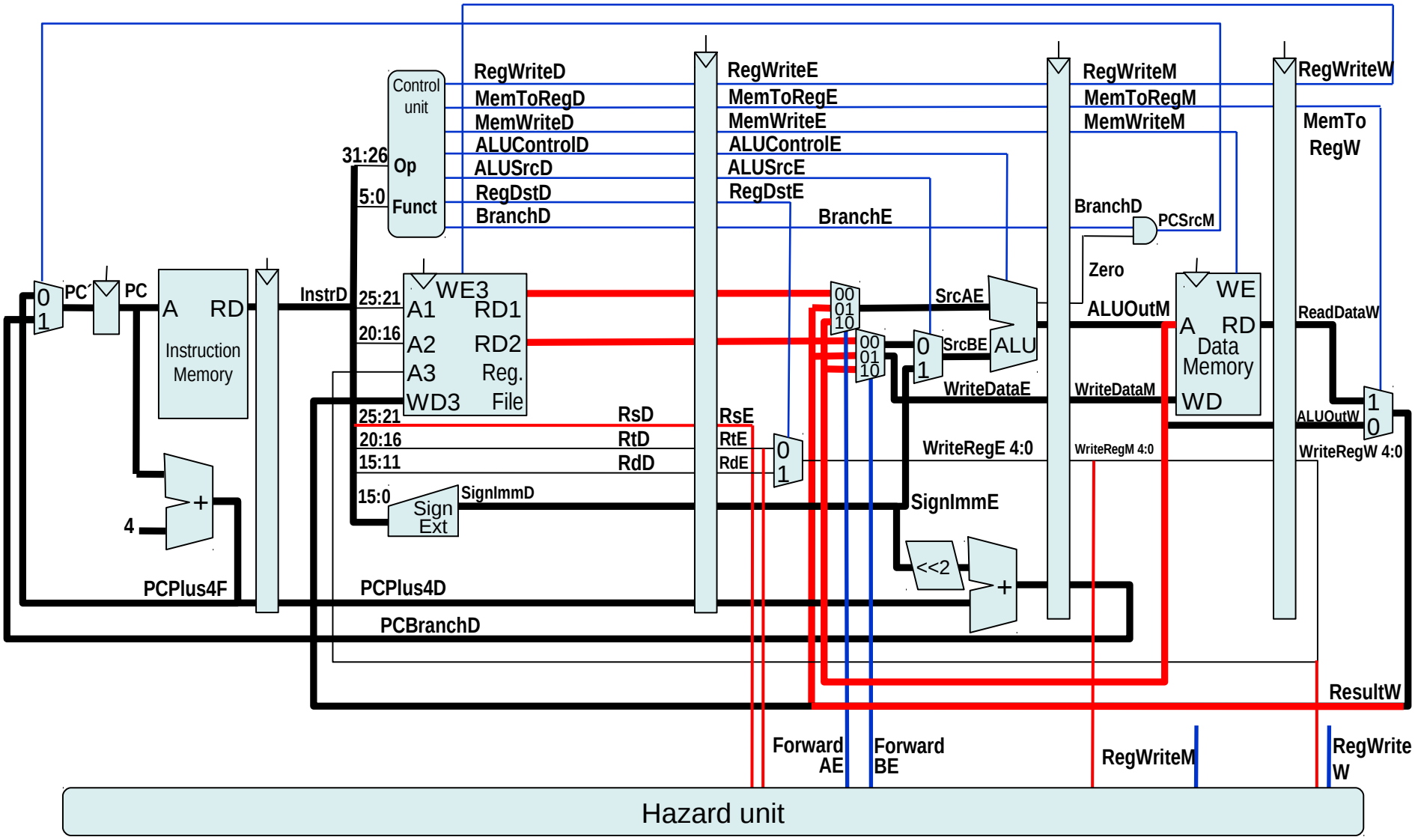


- If a result is available (computed) before subsequent instruction(s) requires the value then data hazard can be avoided by forwarding
- Hazard case is indicated when some of source registers in EX stage is the same as destination register in stage MEM or WB
- The register numbers are fed to the Hazard Unit
- The RegWrite signal from MEM and WB stage has to be monitored as well to check that register number on WriteReg lines takes effect – lw / sw etc.

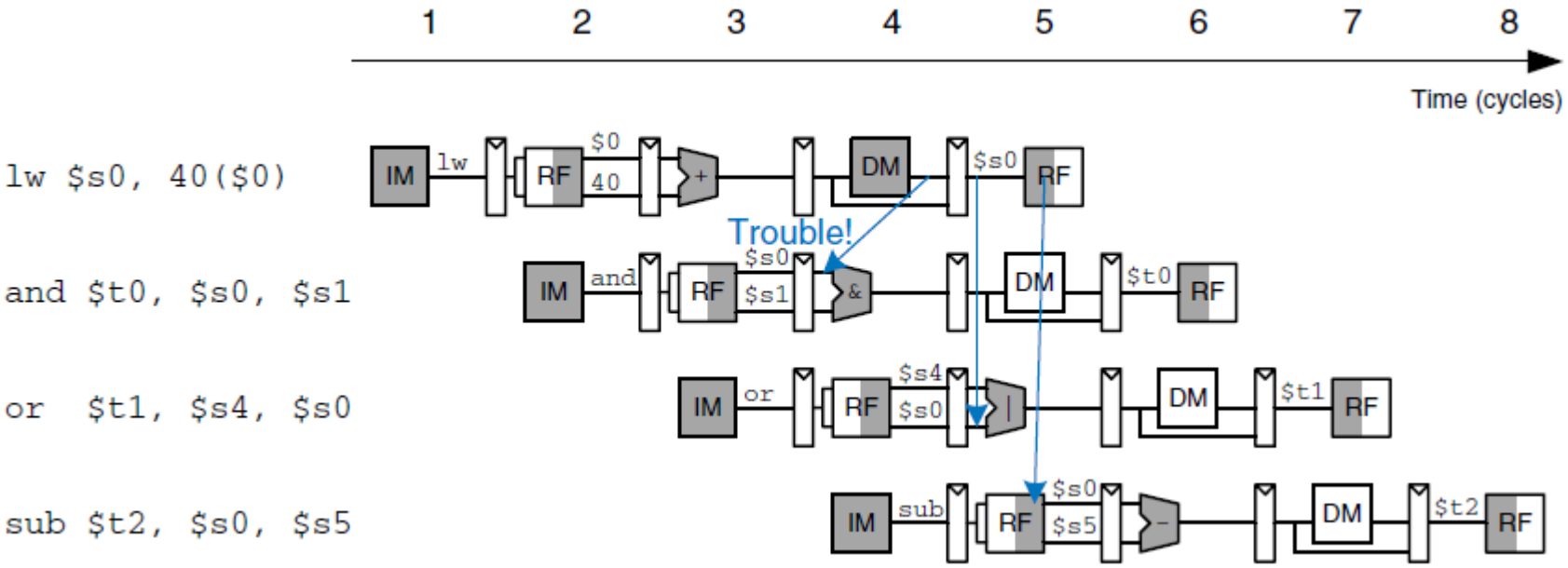
CPU after previous design steps



Data hazards solved by forwarding

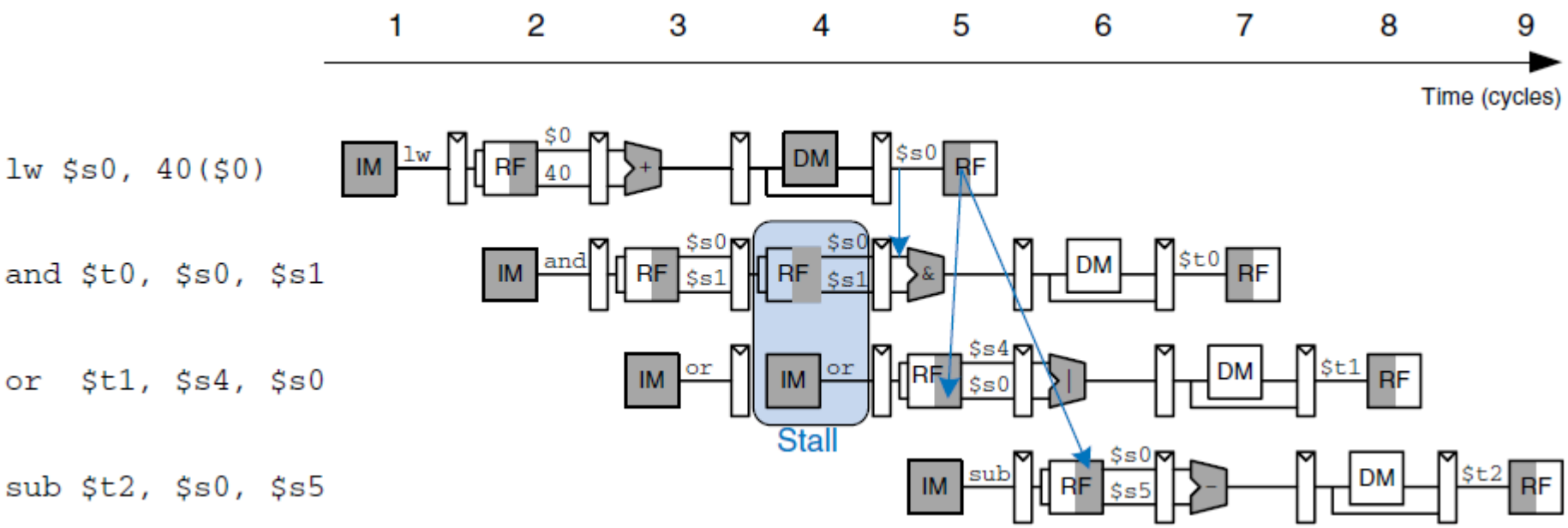


Data hazard avoided by pipeline stall



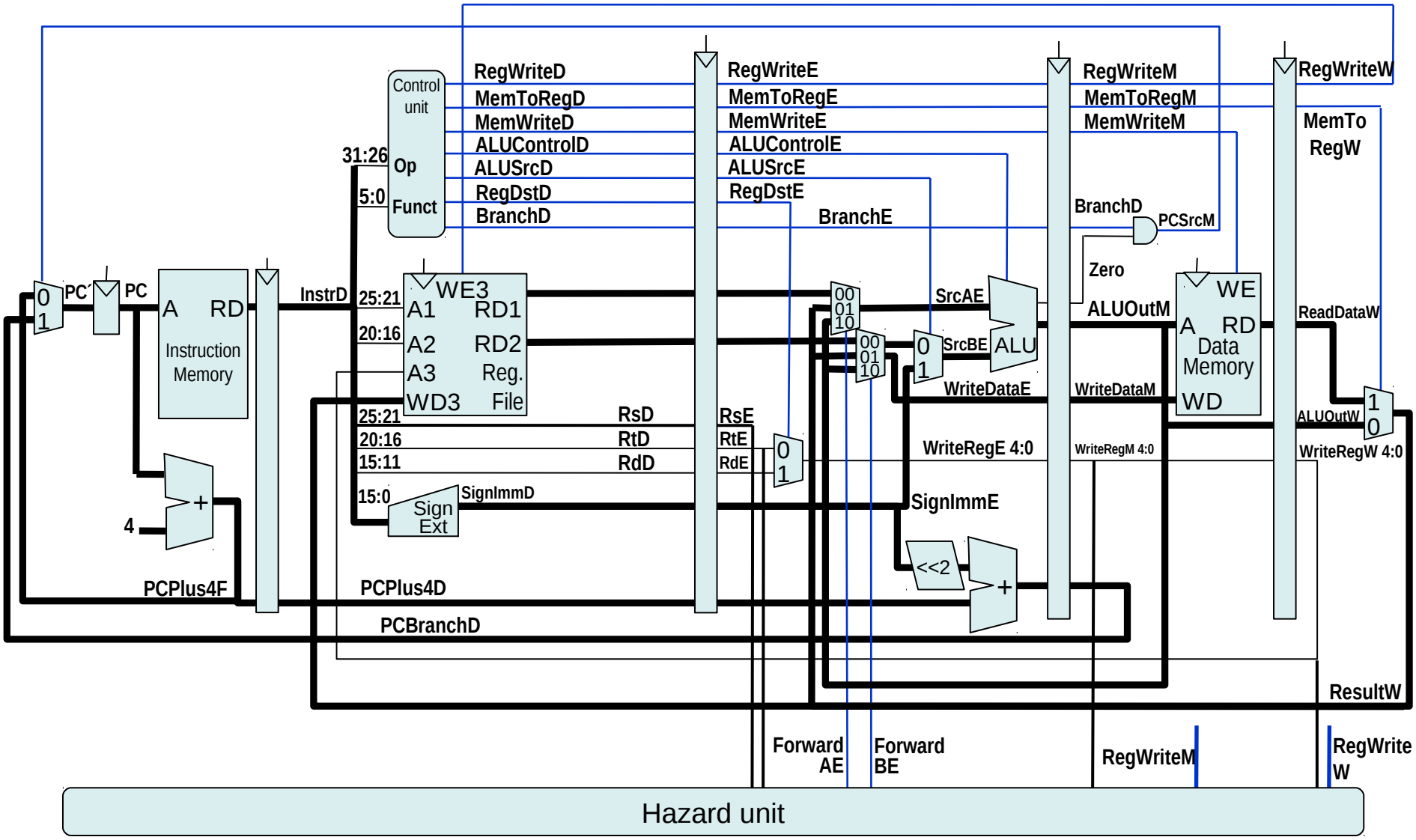
- If subsequent instructions require result before it is available in CPU then the pipeline has to be stalled (stall state inserted)
- The stall is mean to solve hazard but affect system throughput
- Pipeline stages preceding that one which is affected by the hazard are stalled until all results required by subsequent instructions are available – results are forwarded to the sink which required their value

Data hazard avoided by pipeline stall

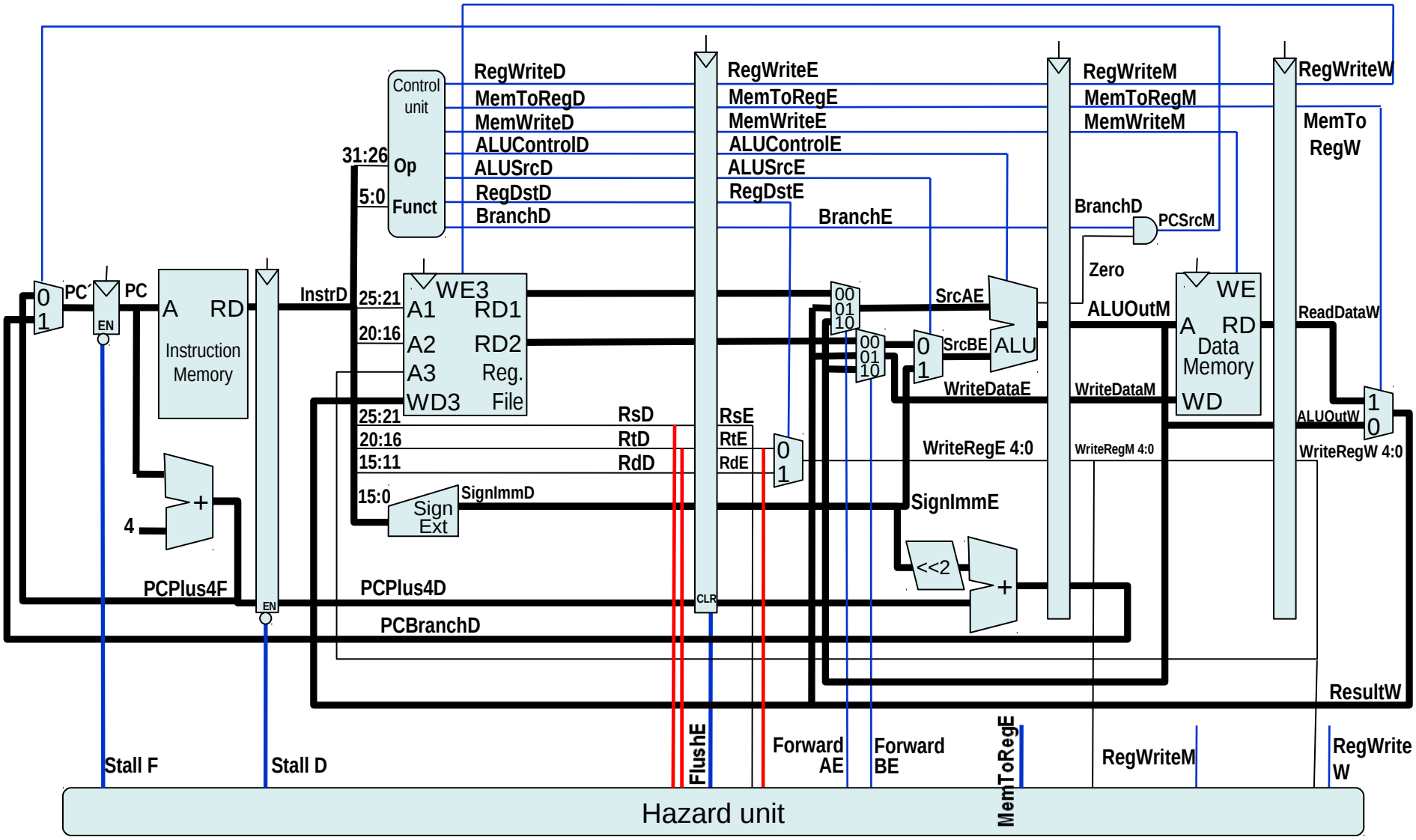


- The stall is realized by the holding content of the inter-stage registers (gating their clocks or blocking their latch enable signals)
- Results from colliding stages have to be „discarded“ – certain control signals in CPU (RF or memory write enable, branch gating) are reset (held low)
- Both is achieved by introduction of control signals to hold and/or reset inter-stages registers

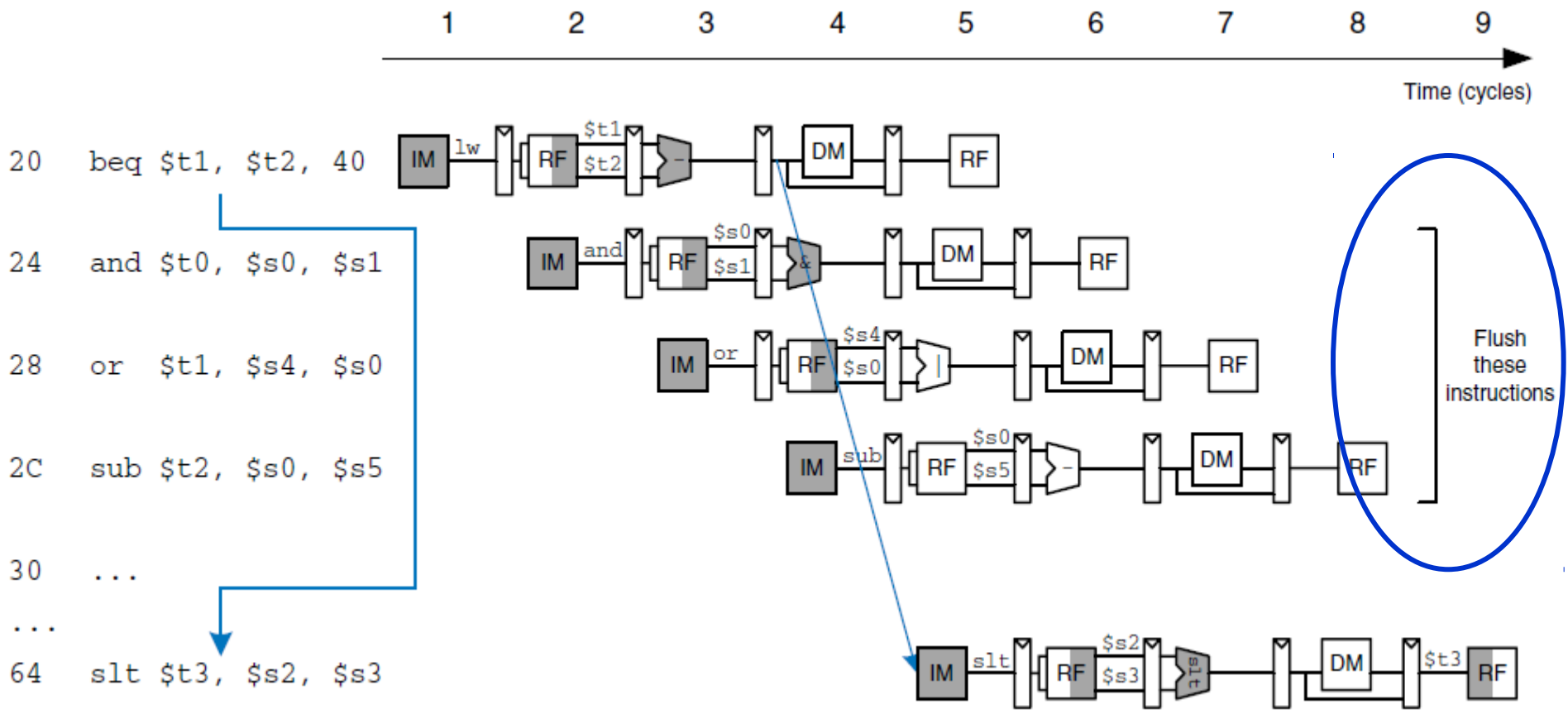
Processor design build till now



Processor with data hazards avoided by stall

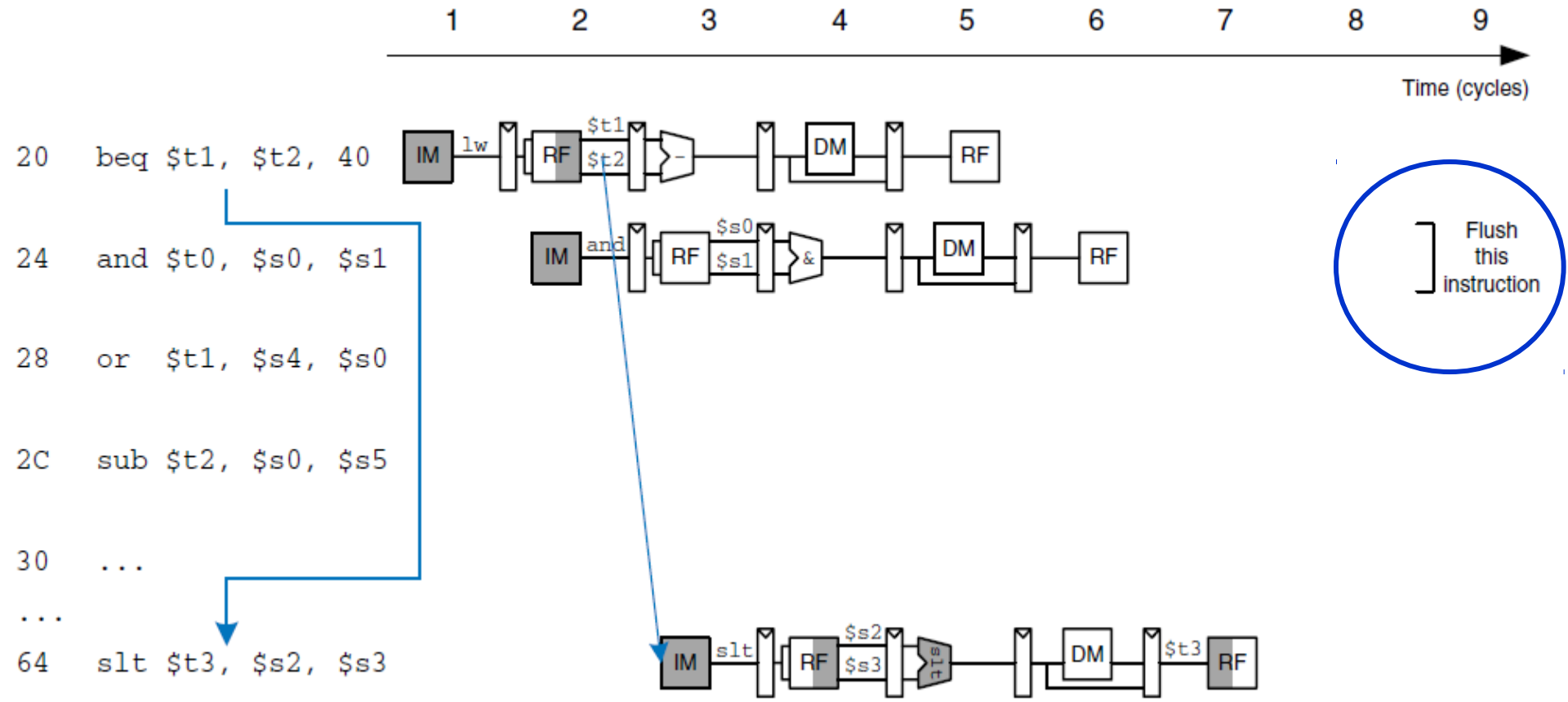


Control hazards (branch and jump)



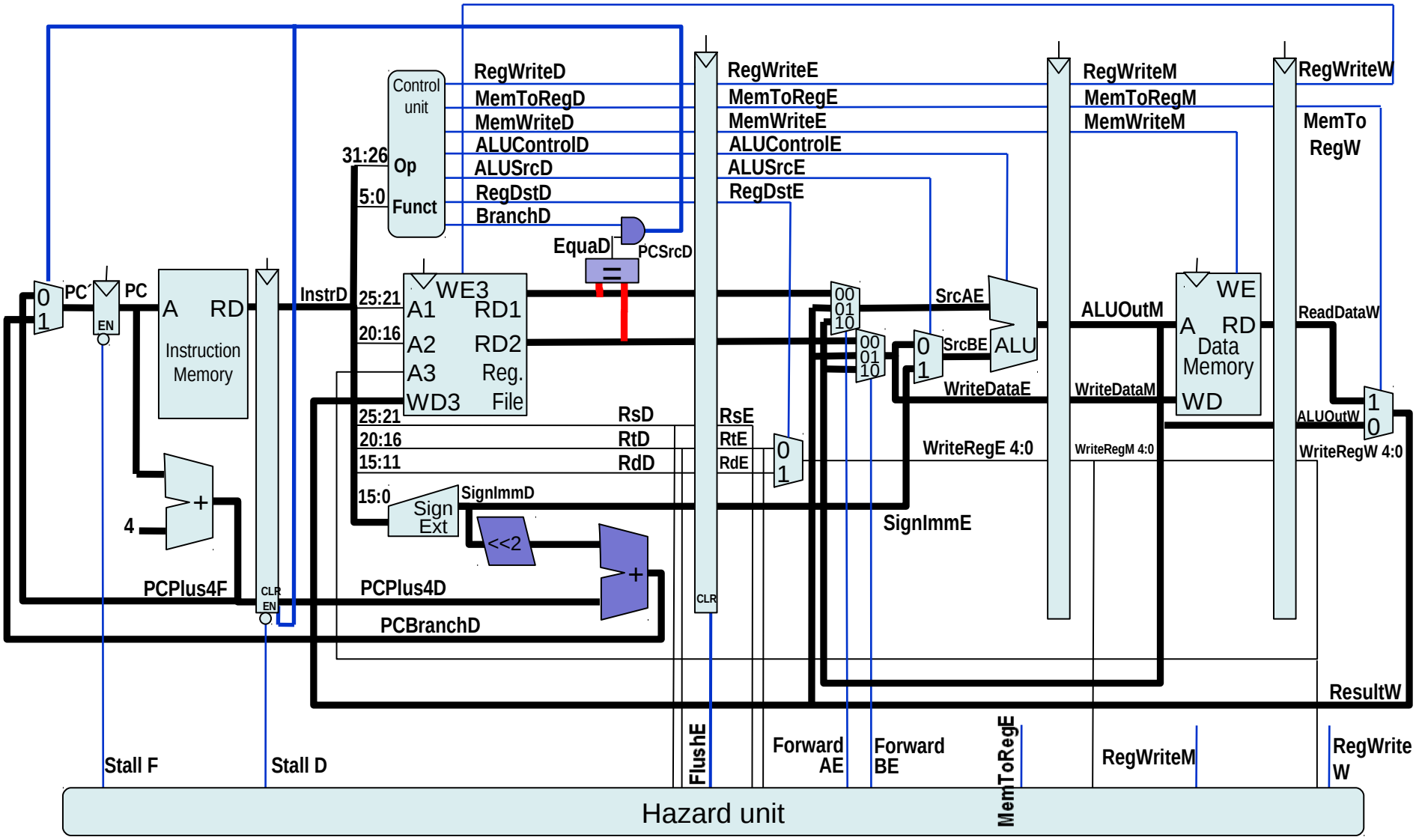
- Result is not known before 4th cycle. Why?

Control hazards – better to know result earlier…

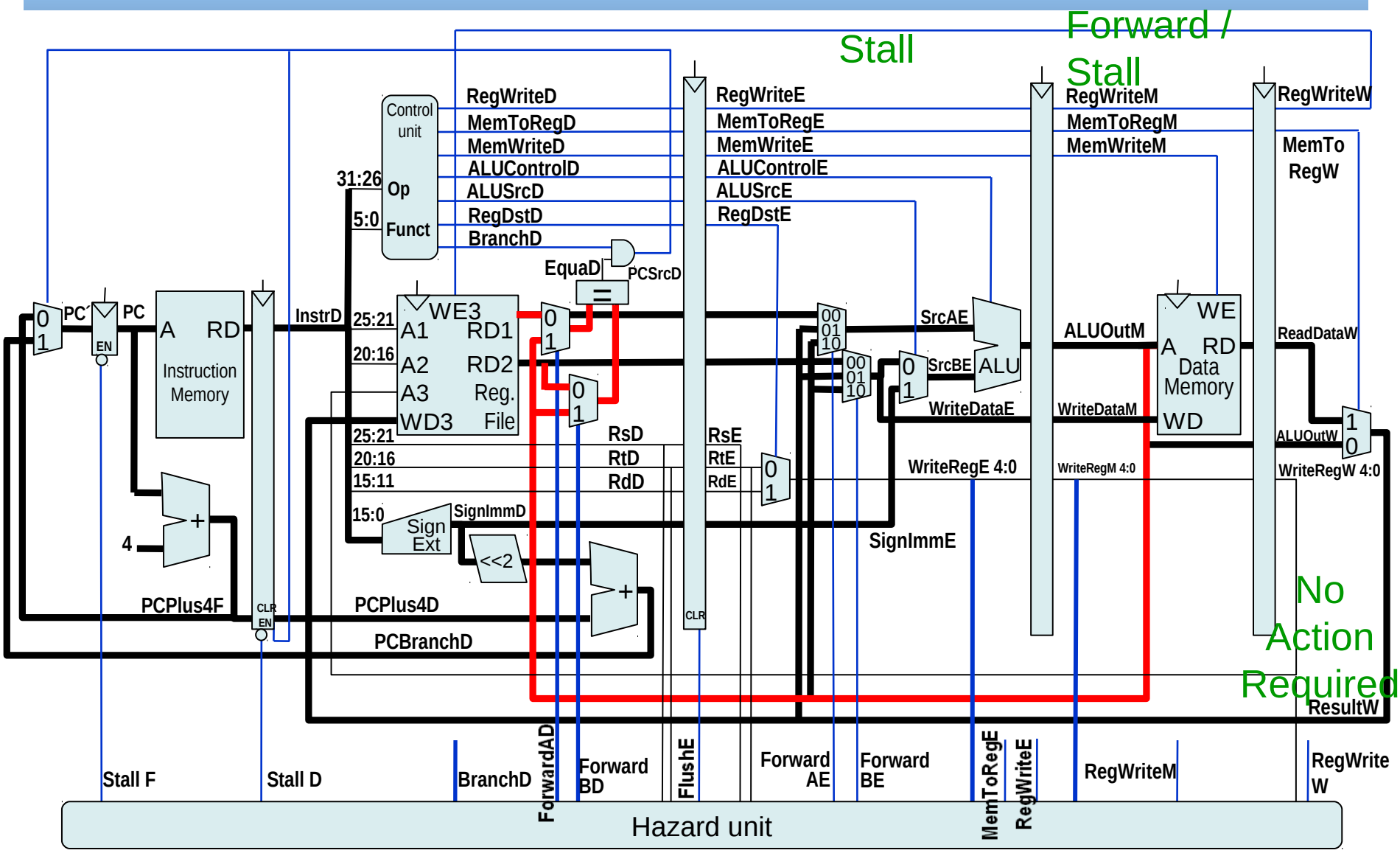


- If the result of comparison can be evaluated in the 2nd cycle **misprediction penalty** can be reduced
- But the processing of the comparison at earlier stage can induce new RAW hazards..!!!

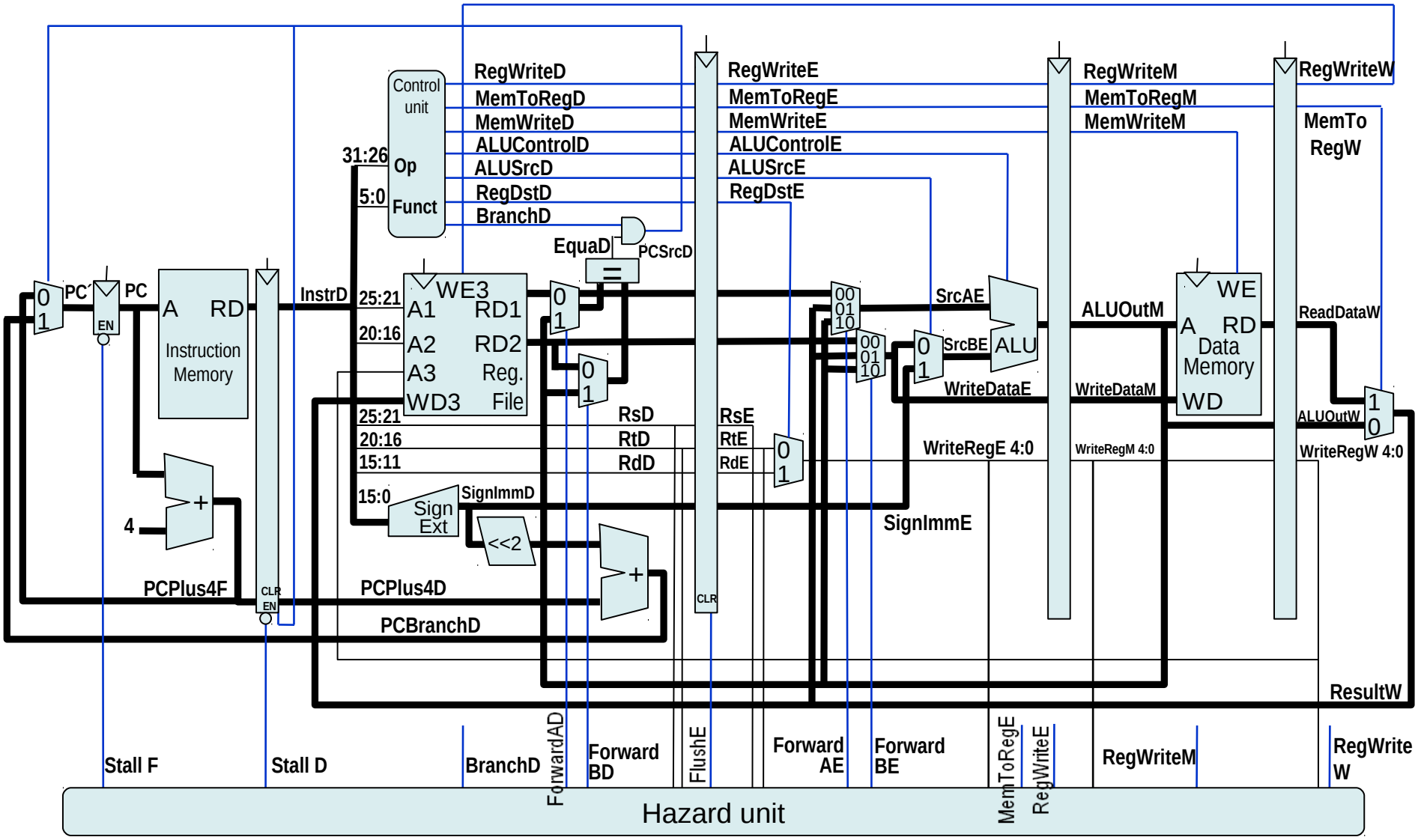
Resolve control hazards by early evaluate and flush



Resolve RAW hazards by forwarding or stalling



We are finished – pipelined processor is designed



Pipelined CPU – performance: IPS = IC / T = $IPC_{avg}.f_{CLK}$

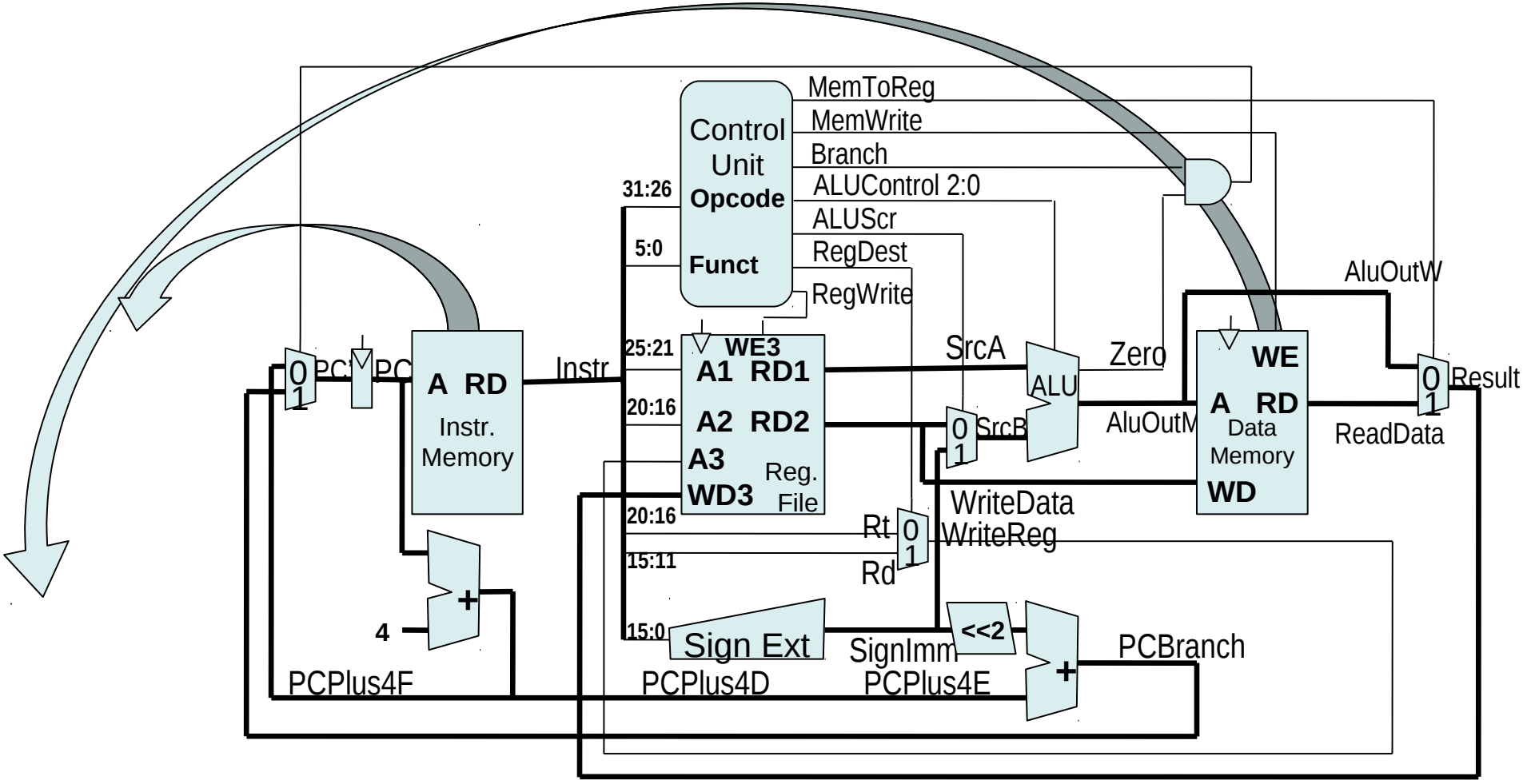
- What is maximal acceptable frequency for the CPU?
- Which stage is the slowest one?
- The cycle time is determined by the slowest stage
- For our case:
  Tc = 300 ns --> 3 333 kHz

  If the pipeline fill overhead is neglected (i.e. no pipeline stalls and flushes are considered) then ideal IPC = 1.
  IPS = 1 • 3 333e3 = 3 333 000 instructions per second

- Introduction of the 5-stage pipeline increases performance (throughput) 3 333 000/ 980 000 = 3.4 times! (considering IPC=1)

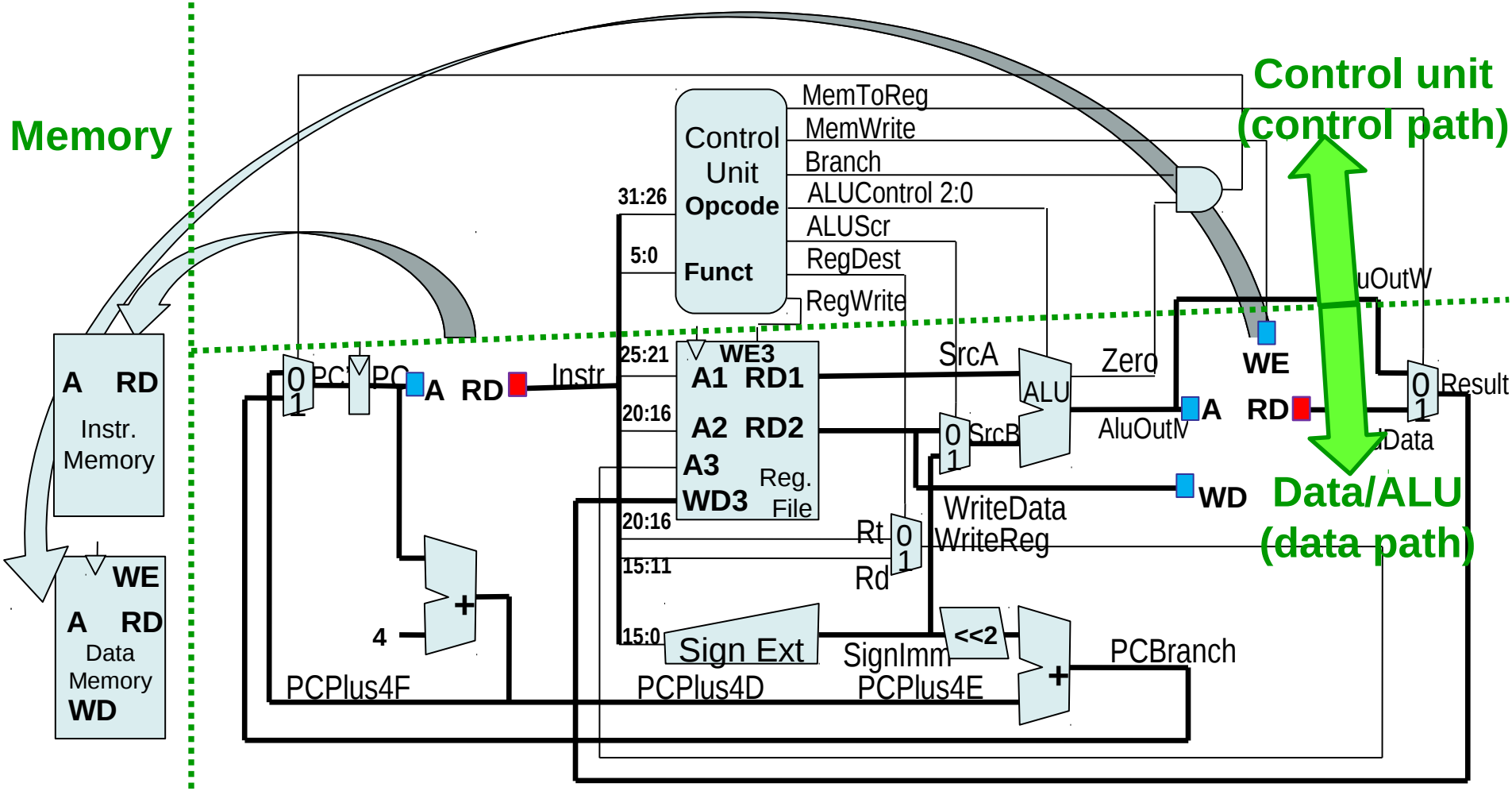
What is result of the design?

Return back to non-pipelined CPU version

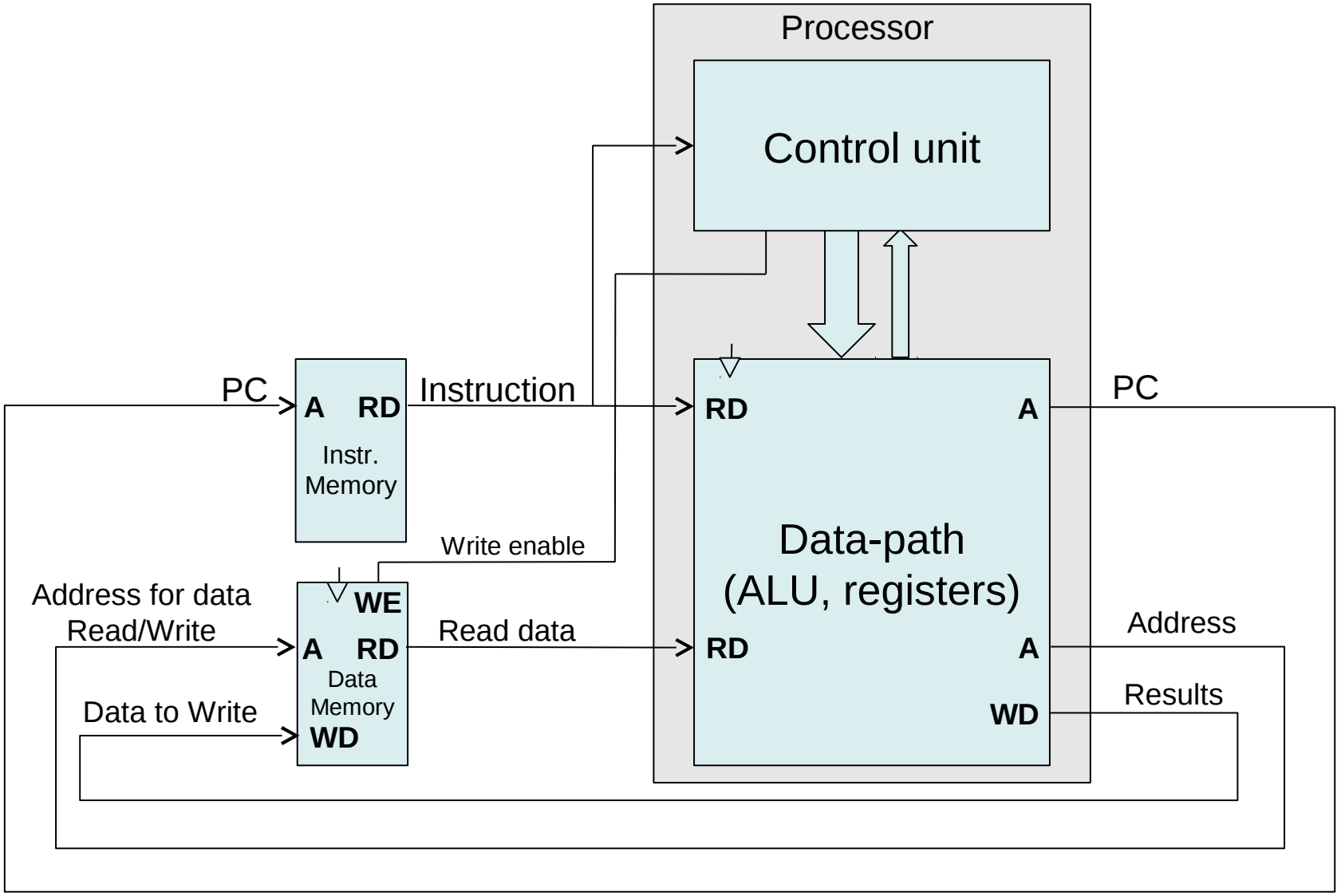


What is result of the design?

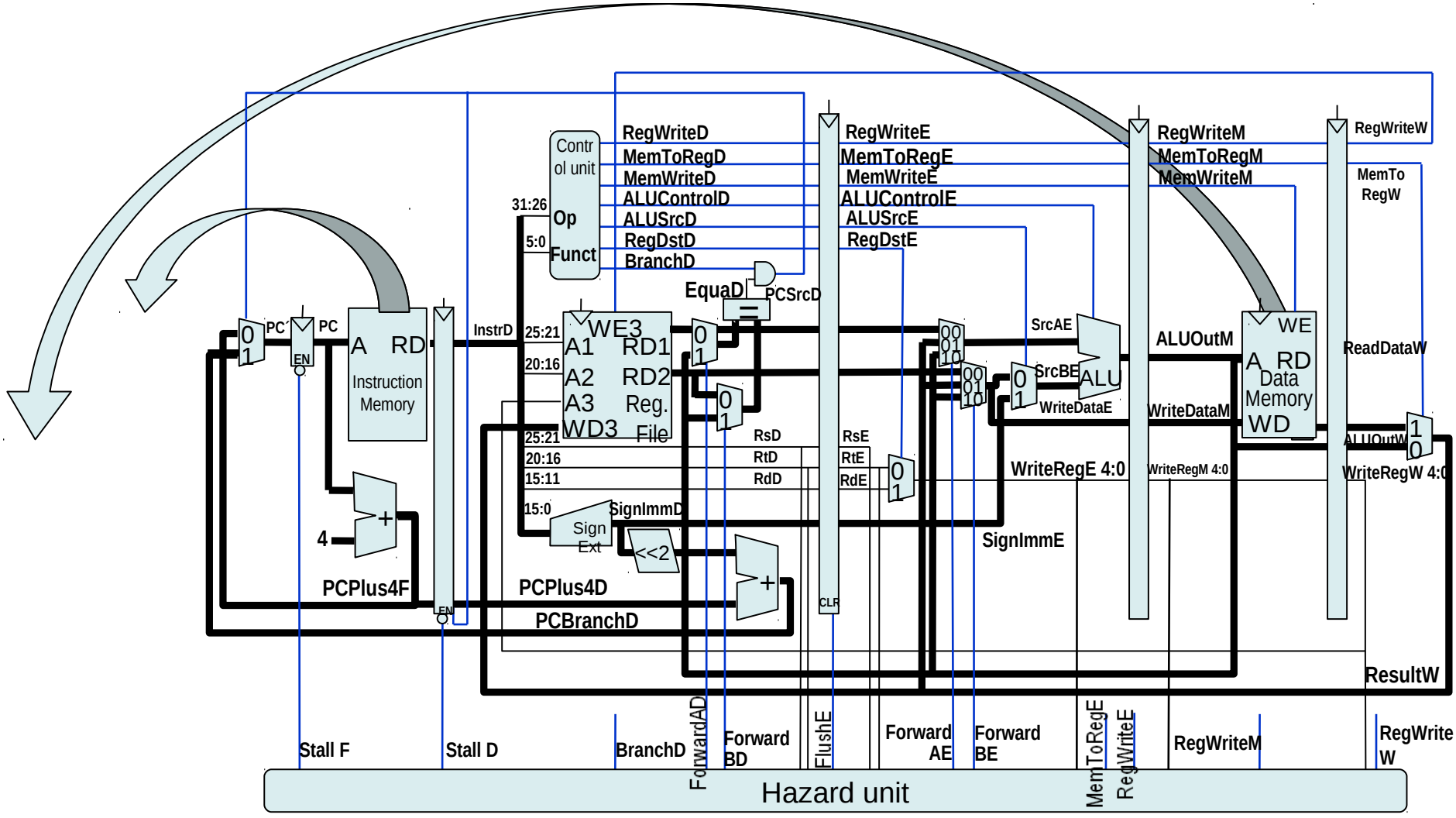
Return back to non-pipelined CPU version



What is result of the design?

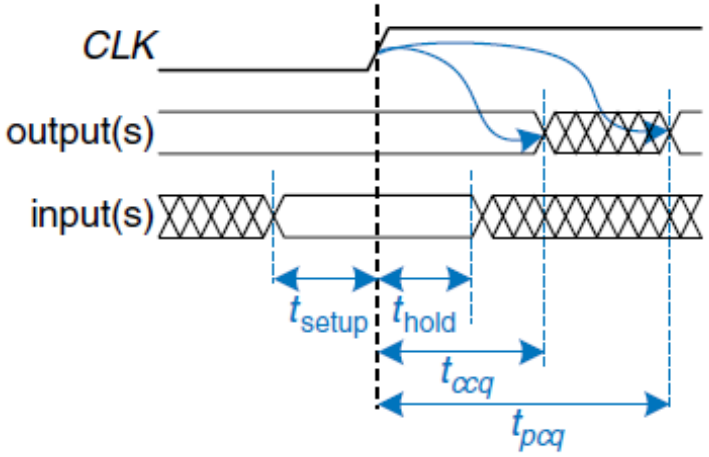


CPU design result – pipelined version



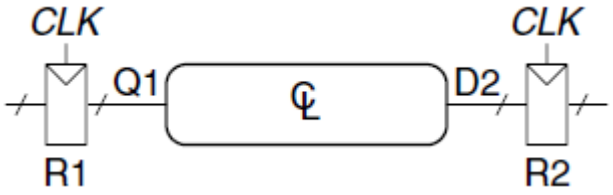
Pipelined CPU – timing

- The timing/AC characteristics of synchronous sequential circuit :

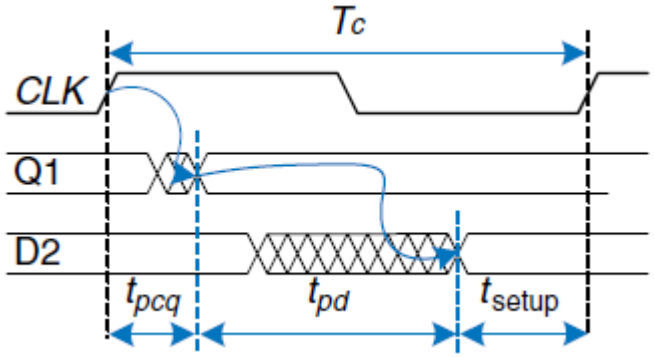


t_{setup} – inputs setup time
t_{hold} – inputs hold time

- Signal integrity constrain for the setup time before the clock:



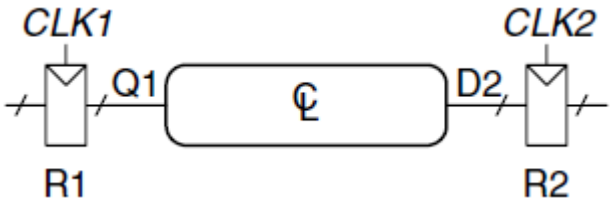
$$Tc >= t_{pcq} + t_{pd} + t_{setup}$$

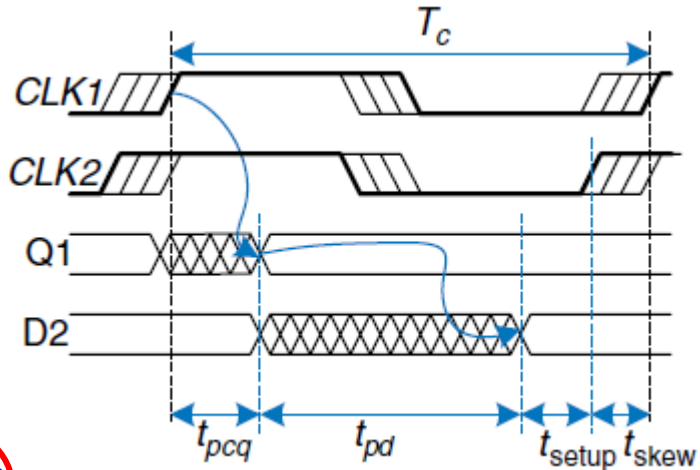


t_{pd} – combinatorial logic propagation delay

Pipelined processor – timing

- Constraint for the setup time (consider the clock distribution jitter):



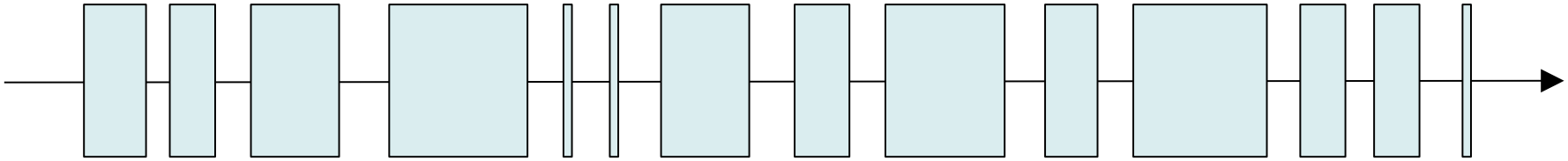


$$Tc >= t_{pcq} + t_{pd} + t_{setup} + t_{skew}$$

Clock distribution jitter is limiting factor,
if it reaches or exceeds value of t_{pd}
(too deep pipeline / too many stages…)

Pipeline stages balancing

Linear pipelining:

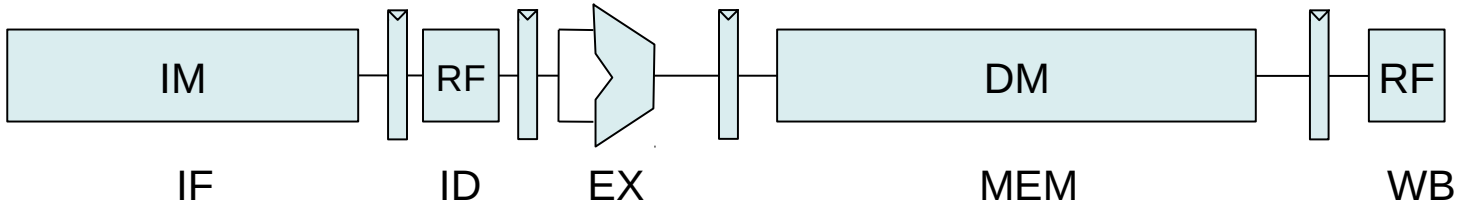


(applies to tree based adder, multiplier, (unrolled) iterative divider..)

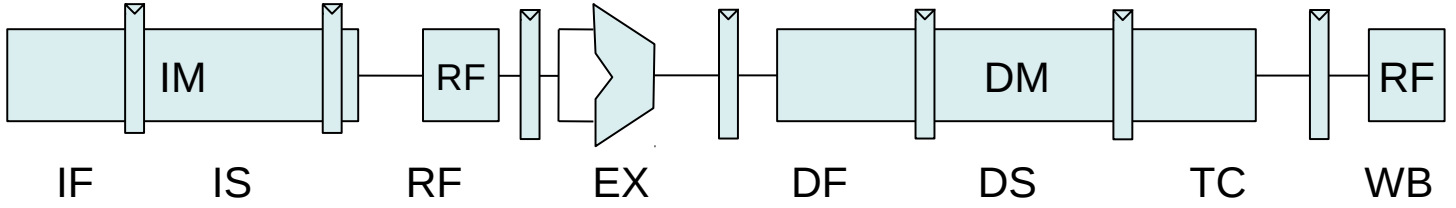
- **Balancing**: the goal is to divide the processing into *N* stages in such way, that stage propagation delays are roughly the same…
- The number of stages reflects preference of performance (throughput) versus latency.

Superpipeline and beyond

- Not well balanced 5-stage pipeline:



- Deeper pipeline is result of decomposing stages into more stages



- It allows CPU to work at higher frequencies but introduces many problems as well..
- Complex forwarding, more pipeline stalls, hazards need to be solved by complex logic