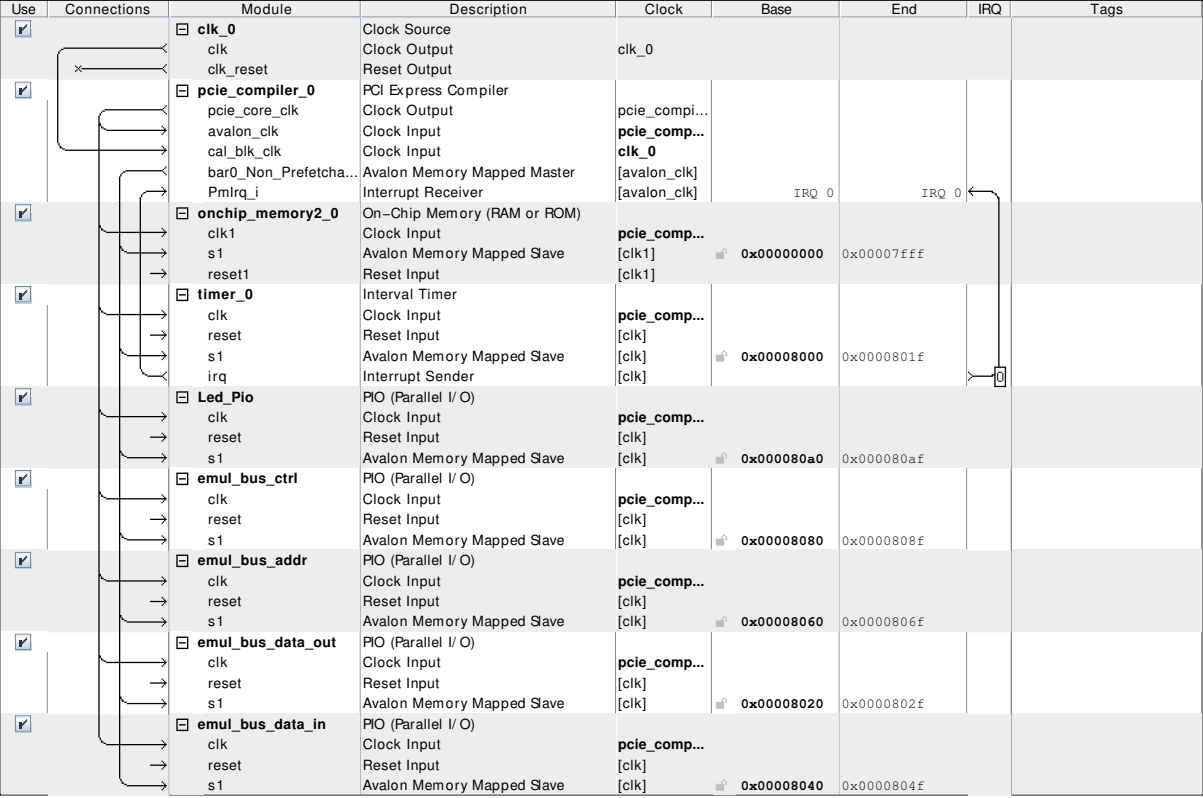

| Use | Connections | Module | Description | Clock | Base | End | IRQ | Tags |
|---|---|---|---|---|---|---|---|---|
| ☑ | | **clk_0** | Clock Source | | | | | |
| | | clk | Clock Output | clk_0 | | | | |
| | | clk_reset | Reset Output | | | | | |
| ☑ | | **pcie_compiler_0** | PCI Express Compiler | | | | | |
| | | pcie_core_clk | Clock Output | pcie_compi... | | | | |
| | | avalon_clk | Clock Input | **pcie_comp...** | | | | |
| | | cal_blk_clk | Clock Input | **clk_0** | | | | |
| | | bar0_Non_Prefetcha... | Avalon Memory Mapped Master | [avalon_clk] | | | | |
| | | Pmlrq_i | Interrupt Receiver | [avalon_clk] | | IRQ 0 | IRQ 0 | |
| ☑ | | **onchip_memory2_0** | On-Chip Memory (RAM or ROM) | | | | | |
| | | clk1 | Clock Input | **pcie_comp...** | | | | |
| | | s1 | Avalon Memory Mapped Slave | [clk1] | **0x00000000** | 0x00007fff | | |
| | | reset1 | Reset Input | [clk1] | | | | |
| ☑ | | **timer_0** | Interval Timer | | | | | |
| | | clk | Clock Input | **pcie_comp...** | | | | |
| | | reset | Reset Input | [clk] | | | | |
| | | s1 | Avalon Memory Mapped Slave | [clk] | **0x00008000** | 0x0000801f | | |
| | | irq | Interrupt Sender | [clk] | | | 0 | |
| ☑ | | **Led_Pio** | PIO (Parallel I/O) | | | | | |
| | | clk | Clock Input | **pcie_comp...** | | | | |
| | | reset | Reset Input | [clk] | | | | |
| | | s1 | Avalon Memory Mapped Slave | [clk] | **0x000080a0** | 0x000080af | | |
| ☑ | | **emul_bus_ctrl** | PIO (Parallel I/O) | | | | | |
| | | clk | Clock Input | **pcie_comp...** | | | | |
| | | reset | Reset Input | [clk] | | | | |
| | | s1 | Avalon Memory Mapped Slave | [clk] | **0x00008080** | 0x0000808f | | |
| ☑ | | **emul_bus_addr** | PIO (Parallel I/O) | | | | | |
| | | clk | Clock Input | **pcie_comp...** | | | | |
| | | reset | Reset Input | [clk] | | | | |
| | | s1 | Avalon Memory Mapped Slave | [clk] | **0x00008060** | 0x0000806f | | |
| ☑ | | **emul_bus_data_out** | PIO (Parallel I/O) | | | | | |
| | | clk | Clock Input | **pcie_comp...** | | | | |
| | | reset | Reset Input | [clk] | | | | |
| | | s1 | Avalon Memory Mapped Slave | [clk] | **0x00008020** | 0x0000802f | | |
| ☑ | | **emul_bus_data_in** | PIO (Parallel I/O) | | | | | |
| | | clk | Clock Input | **pcie_comp...** | | | | |
| | | reset | Reset Input | [clk] | | | | |
| | | s1 | Avalon Memory Mapped Slave | [clk] | **0x00008040** | 0x0000804f | | |